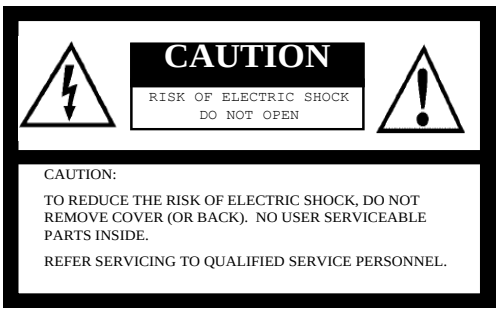
SENTECH

STC-GE33OX
STC-GEC33OX
User Guide

Sentech Power Plus
VGA Color/Monochrome CCD
GigE Vision Camera

Safety Precautions



The lightning flash with arrowhead symbol, within an equilateral triangle, is intended to alert the user to the presence of uninsulated "dangerous voltage" within the product's enclosure that may be of sufficient magnitude to constitute a risk of electric shock to persons.

The exclamation point within an equilateral triangle is intended to alert the user to the presence of important operating and maintenance (servicing) instructions in the literature accompanying the appliance.

For U.S.A.

Warning:

This equipment generates and uses radio frequency energy and if not installed and used properly, I.e., in strict accordance with the instruction manual, may cause harmful interference to radio communications. It has been tested and found to comply with the limits for a Class A computing device pursuant to Subpart J of Part 15 of FCC Rules, which are designed to provide reasonable protection against such interference when operated in a commercial environment.

For Canada

Warning:

This digital apparatus does not exceed the Class A limits for radio noise emissions from digital apparatus set out in the Radio Interference Regulations of the Canadian Department of Communications.

WARNING:

TO PREVENT FIRE OR SHOCK HAZARD, DO NOT EXPOSE THIS APPLIANCE TO RAIN OR MOISTURE.

Product Precautions

- Handle the camera with care. Do not abuse the camera; avoid striking or shaking it. Improper handling or storage could damage the camera.
- Do not pull or damage the camera cable.
- During camera use, do not wrap he unit in any material. This will cause the internal temperature of the unit to increase.
- Do not expose the camera to moisture, or do not try to operate it in wet areas.
- Do not operate the camera beyond its temperature, humidity and power source ratings.
- While the camera is not being used, keep the lens or lens cap on the camera to prevent dust or contamination from getting in the CCD or filter area and scratching or damaging this area.
- Do **not** keep the camera under the following conditions:
    - In wet, moist, and high humidity areas
    - Under hot, direct sunlight
    - In high temperature areas
    - Near an object that releases a strong magnetic or electric field
    - Areas with strong vibrations
- Use a soft cloth to clean the camera. Use pressured air spray to clean the surface of the glass. DO not scratch the surface of the glass.

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Contents

I. Connector Specifications

A. RJ45 Connector

Caution: This is a PoE type product. Apply power (+10.8 to 26.4Vdc) through the power/IO connector whenever PoE is NOT supported.

Pin Assignment

Pin No.	Signal name
1	TA+
2	TA-
3	TB+
4	TC+
5	TC-
6	TB-
7	TD+
8	TD-

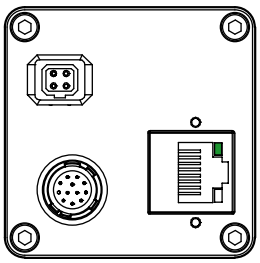
Note: The power supply connection is comprised of PoE (IEEE802.3af)

LED Information

Yellow LED	Green LED	Status
Orange light ON	Green light ON	Power ON
Orange light ON	Green light blinking	1Gb transfering
Light OFF	Green light blinking	100Mb transfering

Power ON the camera

Green LED: Blinking
1Gb Transferring



Yellow LED: OFF
Green LED: Blinking
100Mb Transferring

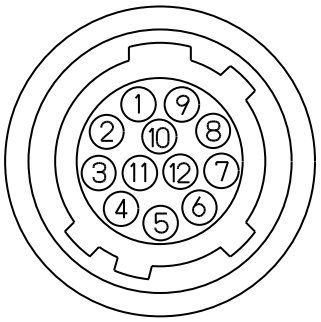
Please use a 1Gb supported NIC, HUB and LAN cable. Check that the NIC and HUB being used is “1Gb transferring”.

Damaging or mishandling the CAT5e cable may cause the transferring speed to change from 1Gb to 100Mb. If this happens, please replace the CAT5e cable.

B. Power/IO Connector
Connector: HR10A-10R-12PB (Hirose) or equivalent
This connector is for DC power input and the input and output signals.

Pin Assignment

No.	Signal type	IO direction	Spec.	Initial signal
1	POWER IN GND	-	GND	-
2	POWER IN	-	+10.8 to 26.4Vdc	-
3	OUT0_AUX_OP	OUT	Opt. Isolated	FrametriggerWait out
4	OUT1_AUX_OP	OUT	Opt. Isolated	ExposureActive out
5	OUT2_AUX_OP	OUT	Opt. Isolated	Open
6	OUT3_AUX_OP	OUT	Opt. Isolated	Open
7	OUT4_AUX_OP	OUT	Opt. Isolated	Open
8	IN0_AUX_OP	IN	Opt. Isolated	TRG In
9	IN1_AUX_OP	IN	Opt. Isolated	Open
10	IN2_AUX_OP	IN	Opt. Isolated	Open
11	IO VCC IN	-	IO VCC +3 to +26.4Vdc	-
12	IO GND	-	IO GND Refer Fig. 3	-



Notes:
- All I/Os (Pin numbers 3 through 10) are user assignable.
- Do NOT connect or disconnect the power/IO connector while the power is being input through the PoE.

1. Input Signal
TRG IN: Input the trigger signal
High: Voltage of the 'IO VCC IN'
Low: Smaller than 0.4V

2. Output Signals
Set the output signals from the power/IO connector.
The following six output signals are selectable with the software or communication.

a. FrameTriggerWait
This function allows the user to check the camera's conditions (the camera exposure and the image output processing by the trigger signal).

1) High Status (Voltage of the "IO VCC IN"): No processing by the trigger signal. The camera accepts the trigger signal.
2) Low Status (0V): The camera exposure and image output is processed by the trigger signal.

The camera's default setting is set so that the trigger signal is INVALID while during the low status of this signal.
In order to start the exposure while the image is being output by the next trigger signal, please change the camera settings (Device code: 001, Command: 13H) to accept the trigger signal while the image is being output.
Noise may appear on the image when the exposure is initiated while the image is being output. In this case, please change the "H reset" of the exposure start mode (Device code: 00H, Command: 12H) in order to change the exposure start point to the next HD timing.

b. UserOutput
The status of the User Output signal can be changed with the "UserOutputValue".

c. ExposureActive
The user can check the exposure time with the ExposureActive signal.

1) High Status (Voltage of the "IO VCC IN"): The camera is exposing
2) Low Status (0V): The camera is not exposed

d. TriggerAuxiliary
This TriggerAuxiliary signal is the input trigger signal.

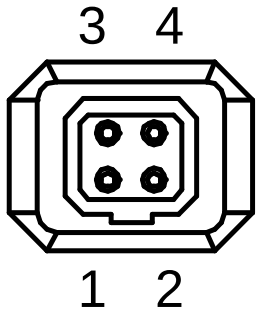
e. TriggerInternal
This TriggerInternal signal is the input trigger signal with the trigger delay time.

f. SensorReadOut
This SensorReadOut signal is the FVAL signal, which is the image output period of the time.

C. DC IRIS Lens Connector
Connector: M1951 (EMUDEN) or equivalent

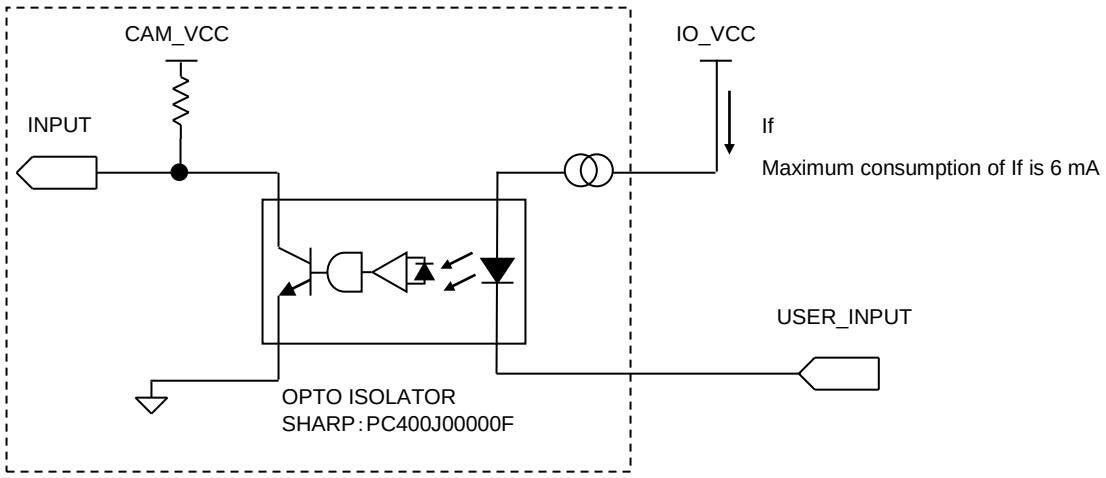
Pin Assignment

Pin No.	Signal name
1	DAMP-
2	DAMP+
3	DRIVE+
4	DRIVE-

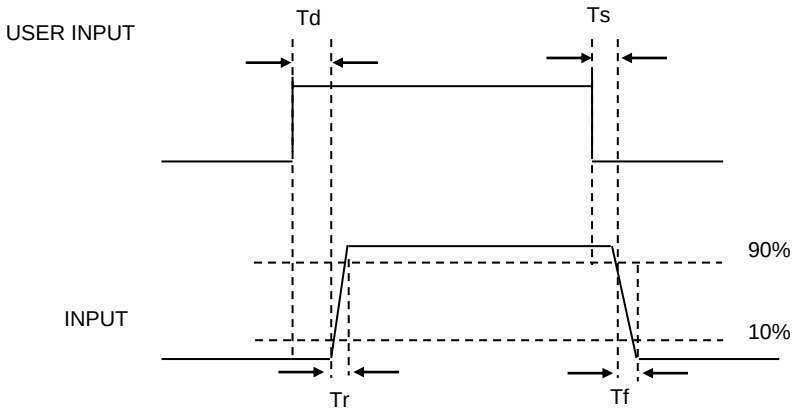


II. I/O Circuits

A. Input Circuit

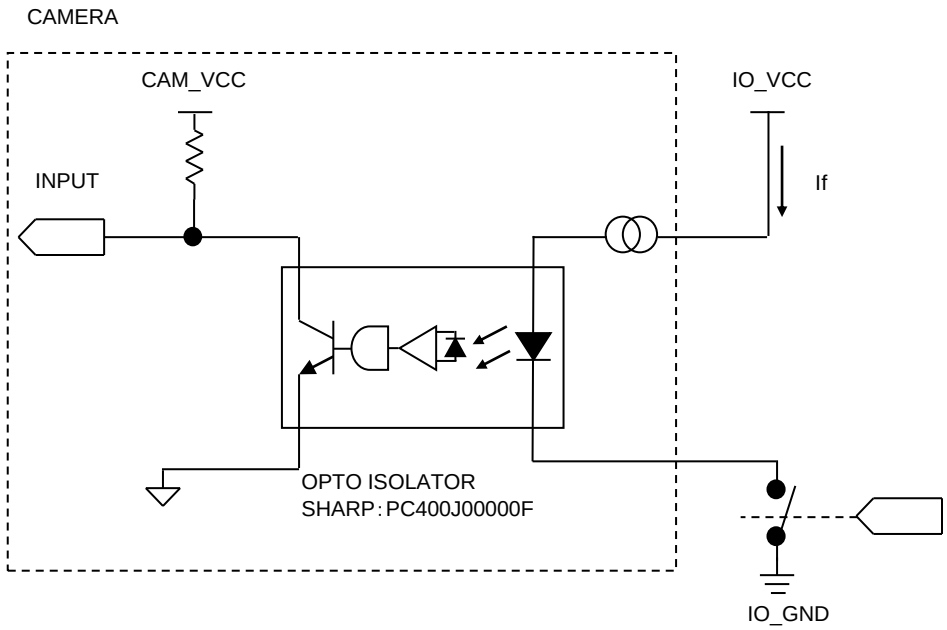


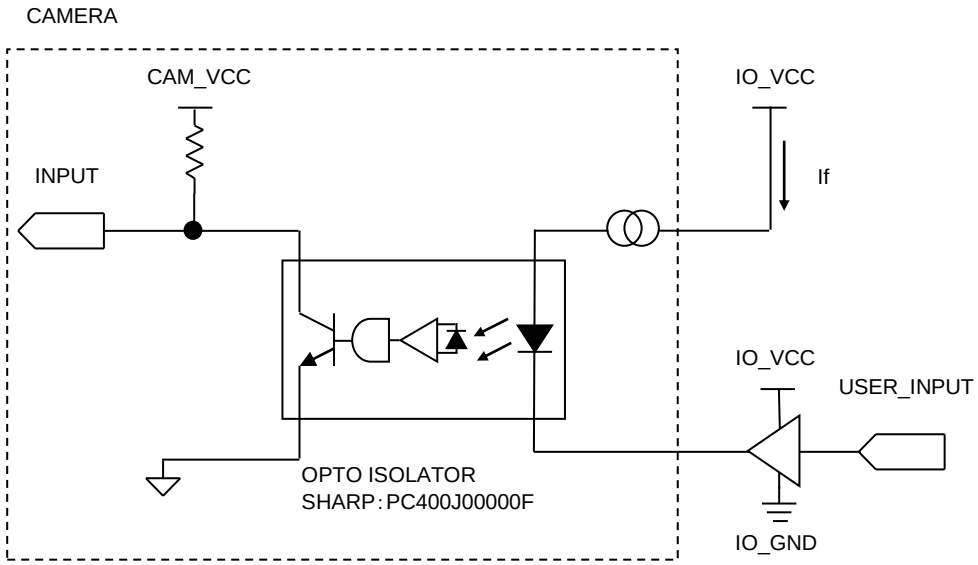
Response Timing



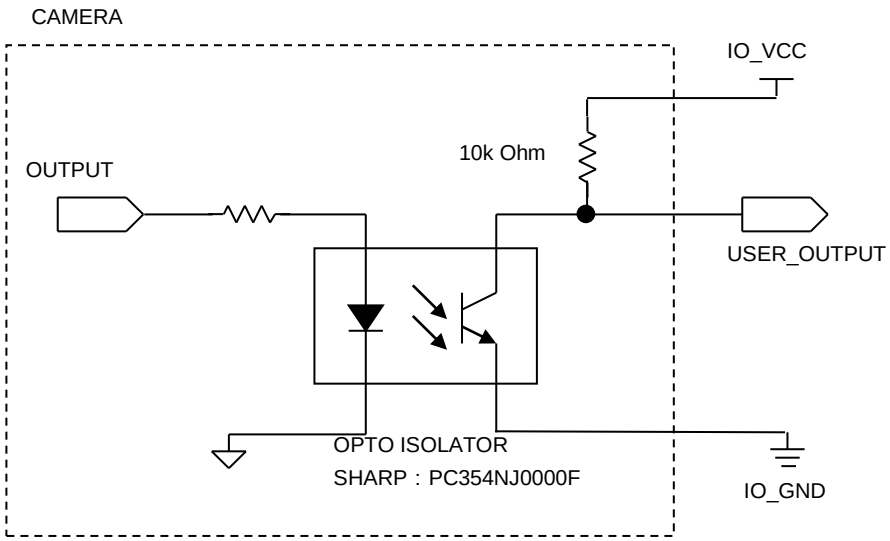
	IO VCC			
	3.3[V]	5.0[V]	12[V]	24[V]
Td	2.5[us]	2.8[us]	3.0[us]	3.0[us]
Tr	100[ns]	100[ns]	100[ns]	100[ns]
Ts	689[ns]	584[ns]	545[ns]	520[ns]
Tf	11[ns]	11[ns]	11[ns]	11[ns]

Example Circuit for the Input Signal

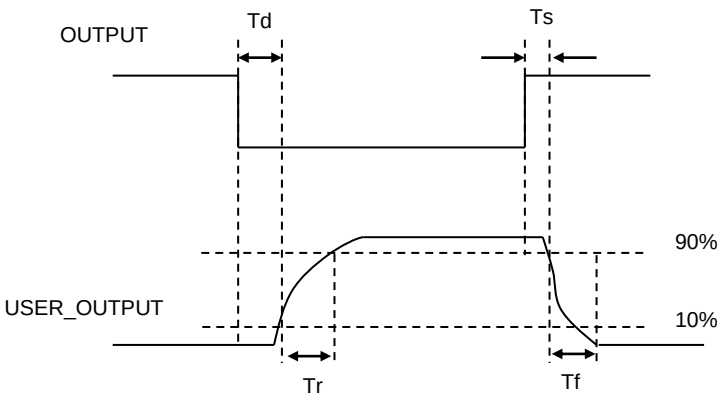




B. Output Circuit



Response Timing



	IO VCC			
	3.3[V]	5.0[V]	12[V]	24[V]
Td	29.6[us]	30.4[us]	35.2[us]	28.4[us]
Tr	67.5[ns]	60.2[ns]	42.3[ns]	31.0[ns]
Ts	2.2[ns]	2.2[ns]	2.8[ns]	2.8[ns]
Tf	3.1[ns]	3.8[ns]	6.9[ns]	10.9[ns]

III. User Configurable FPGA (XILINX)

The customer would program the provided FPGA (XILINX) with its own proprietary code and the customer would also have complete control over 'memory' utilization.

A. User Configurable FPGA (XILINX) Information

1. Device Information

The manufacturer names and item numbers of the user configurable FPGA and the peripheral devices are listed in the following table:

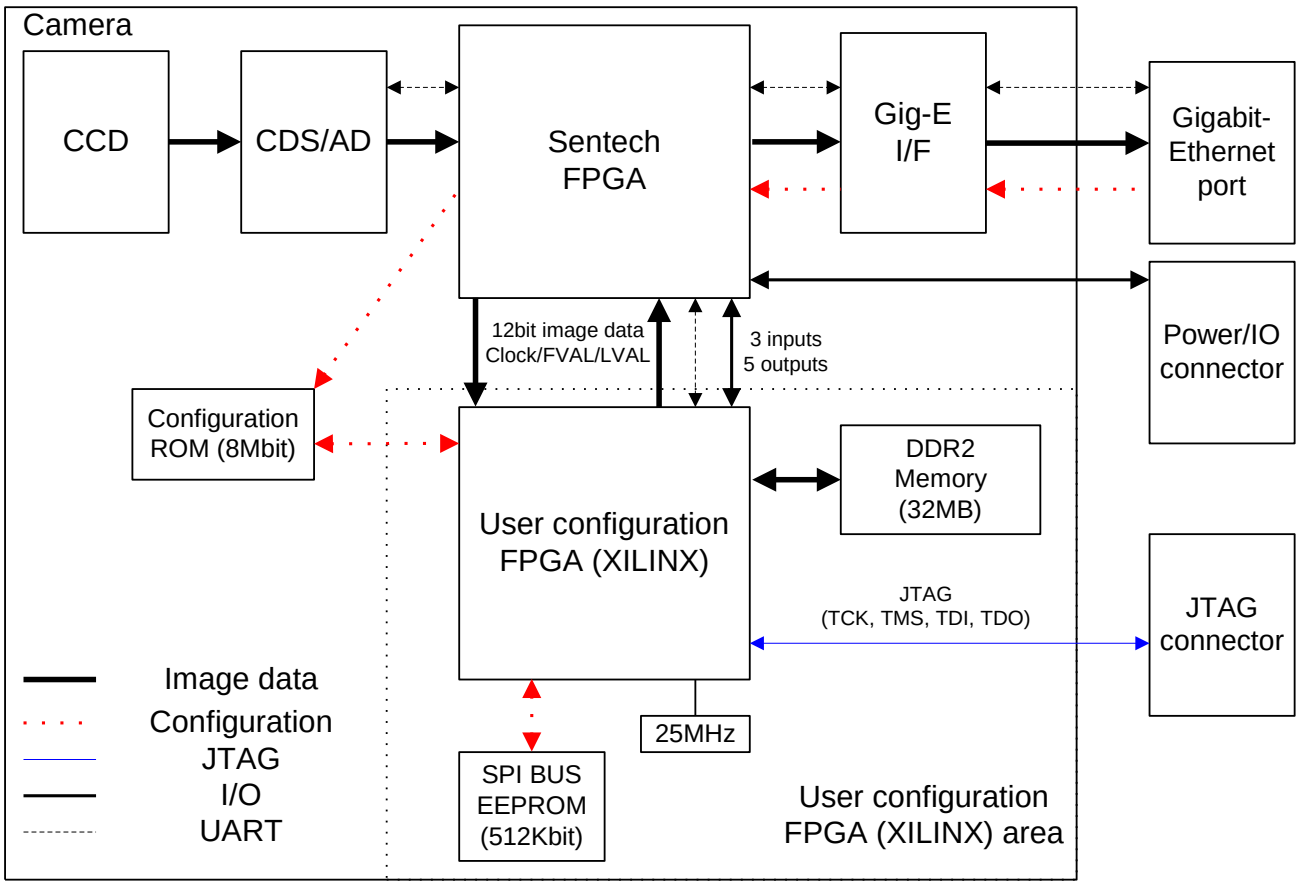
Device	Part number	Size	Manufacture
FPGA	XC3SD1800A (Package: CSG484)	1800 k gate	XILINX
DDR2	W9725G6JB-25	32 MB	Winbond
EEPROM	M95512-RMN6TP	512 kbit	ST Micro
Configuration ROM	M25P80-VMP6G	8 Mbit	Micron

2. User Program Examples

Implementation of proprietary algorithm
Image processing and conversion
Image storage
Image analysis
Pattern comparison and others

B. Block Diagram and Explanation

1. Block Diagram



2. Explanations of Data Flows

a. Image Data

1) Image Data Flow

a) The analog image signal crated by the CCD is processed through the CDS (Correlated Double Sampling) section and then is converted into digital data by the A/D converter.

b) This data is then sent to the “Sentech FPGA” for further processing.

c) Once the data is sent into the “Sentech FPGA”, the image can then be routed to the “User Configurable FPGA”. For this, there are three different extraction points in the “Sentech FPGA”; please see the following section for more information.

d) This data is then further processed by the program created by the user in the “User Configurable FPGA”.

e) Now the data should be returned to the “Sentech FPGA”. In this process there are, again, three different points within the “Sentech FPGA” to return the data to. Please see the following section for more information.

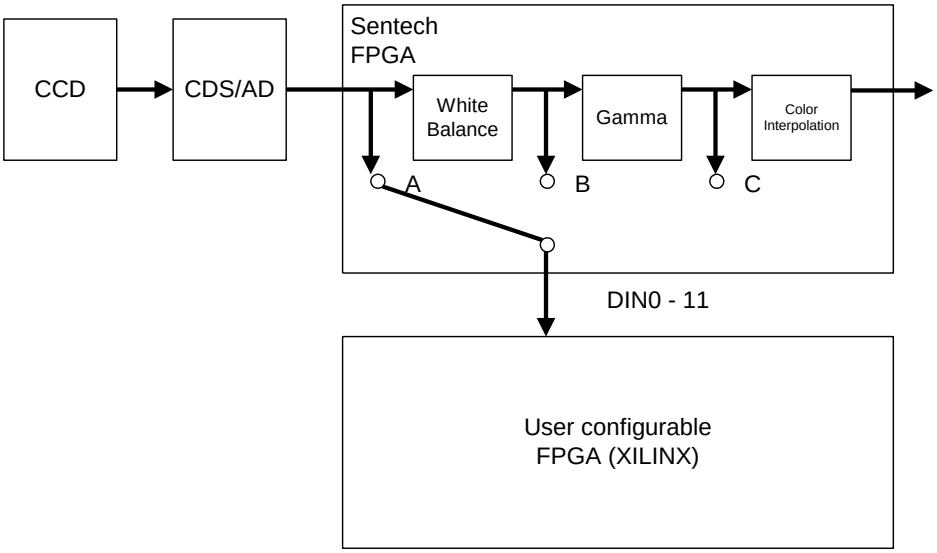
f) The data is sent to “GigE I/F (Interface)” and sent out through the Ethernet connector.

2) Image Data Extraction and Insertion

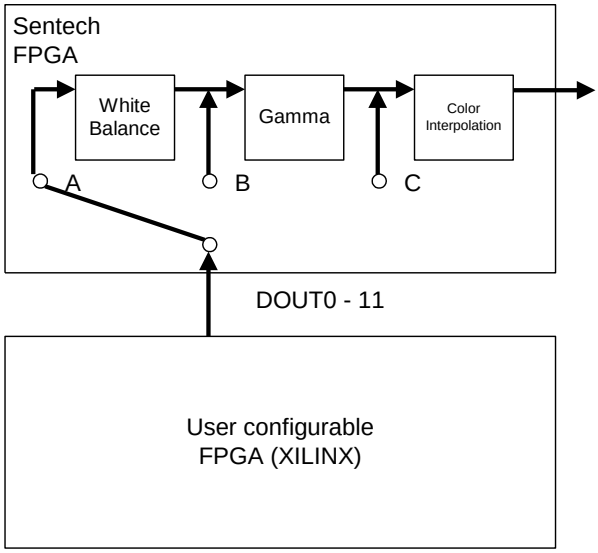
Image data generated by the CCD is converted into 12-bit digital data. This data is extracted into the user FPGA, processed and inserted back to the Sentech FPGA.

a) Image Data Flow Block Diagram

The image data from Sentech FPGA to user configurable FPGA



The image data from user configurable FPGA to Sentch FPGA



b) Data Extraction from the Sentech FPGA

The 12-bit image data is extracted from the Sentech FPGA as DIN11-0 into the user FPGA from any points listed below. These points A, B and C are indicated in the Image Data Flow Block diagram on the previous page.

- For Color Cameras:
  A. CCD Raw Data
  B. Data after the white balance processing
  C. Data after the white balance and gamma processing
- For Monochrome Cameras:
  A or B. CCD Raw Data
  C. Data after the gamma processing

c) Data Extraction from the User Configurable FPGA

After processing the 12-bit image data in the user FPGA, the data is inserted back to the Sentech FPGA as DOUT11-0 at any of the following points listed below. These points A, B, and C are indicated in the Image Data Flow Block diagram on the previous page.

- For Color Cameras:
  A. The gamma and color interpolation processing prior to the white balance
  B. Prior to the gamma and color interpolation processing
  C. Prior to the color interpolation processing
- For Monochrome Cameras:
  A or B. Prior to the gamma processing
  C. Prior to the camera output (No processing)

d) Data Assignment List

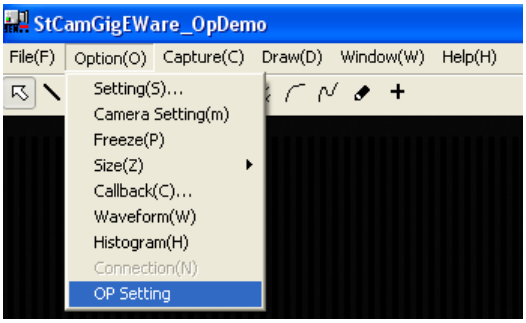
Please refer to Section III-C for the data assignment.
Note: It is not necessary to use these data pin assignments in section III-C if the user is using the pin assignment and the timing constraint files (Power_plus_000.ucf).

e) Image Data Switching Method

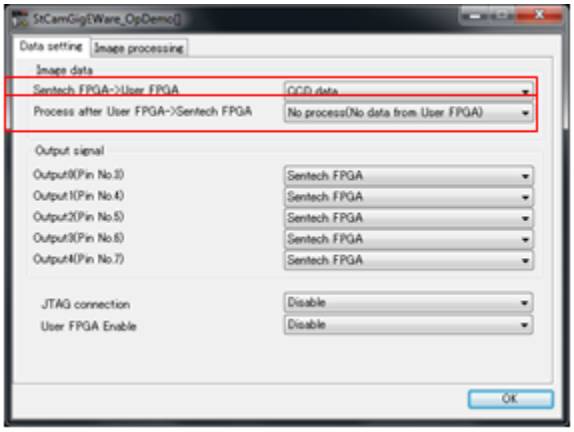
As previously explained in section III-B-2-a-2, there are three points to extract the image data from the Sentech FPGA and the image process at the Sentech FPGA after the image data is sent back from the user configurable FPGA. There are two different methods to achieving this switch:

1) By using the Sentech GUI “StCamGigEWare_OpDemo”
   Please refer to the “User Configurable FPGA (XILINX) Sample Codes”

   a. Select “OP Setting” under “Option” in the menu.



b. Select which image data to send from the “Sentech FPGA” to the “User Configurable FPGA” at “Sentech FPGA -> User FPGA”.



Selection	Image data from Sentech FPGA	
	Color camera	Monochrome camera
CCD data	CCD raw data	CCD raw data
White balance processed data	White balance processed image data	CCD raw data
White balance and gamma processed data	White balance processed and gamma processed image data	Gamma processed image data

c. Under “Process after User FPGA -> Sentech FPGA”, the user can select the type image process at the Sentech FPGA after the image data is sent back from the “User Configurable FPGQA”.

Selection	Image process at Sentech FPGA after the image data send back from User FPGA	
	Color camera	Monochrome camera
No process	No image data from the User FPGA	No image data from the User FPGA
White balance, gamma and color interpolation	White balance, gamma and color interpolation processing	Gamma processing
Gamma and color interpolation	Gamma and color interpolation processing	Gamma processing
Color interpolation	color interpolation processing	No processing

2) By Changing the Register Value through the UART.
Also, please see section VI “The Communication Protocol Specifications”.

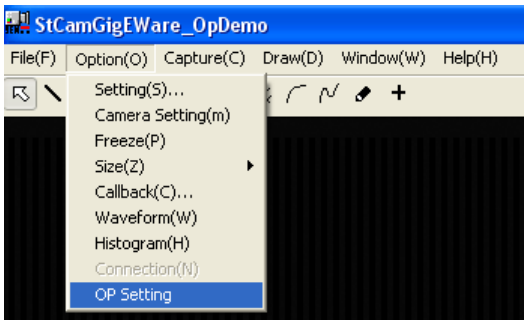
a. Set the image data between FPGAs (Device code: 20H, command: C0H).

b. Configuration Data

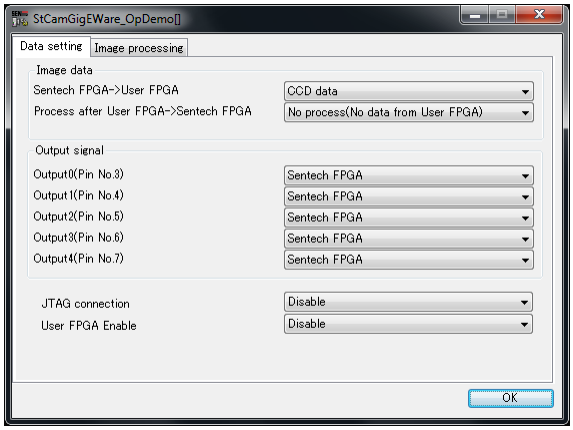
1) The FPGA program created by the user is sent to the “Configuration ROM” through the Ethernet connector as the “Configuration data”.
2) The data is sent through the “GigE I/F” and “Sentech FPGA” to “Configuration ROM” and stored.
Note: Please see the “User configurable FPGA (XILINX) uploading instructions” for more detailed information.
3) Select “Enable” at the “User FPGA Enable” whenever the user configurable FPGA has to configure with the uploaded configure data for the user configurable FPGA.
The user configurable FPGA does not work if “Disable” is selected at the “User FPGA Enable”.

a) By using Sentech GUI “StCamGigEWare_OpDemo”
Please refer to “User Configurable FPGA (XILINX) Sample Codes for more information

Select “OP Setting” under “Option” in the menu.



1) Select what image data is sent from “Sentech FPGA” to “User Configurable FPGA” at “Sentech FPGA -> User FPGA”.



b) By changing the register value through the UART
Please refer to section VI. The Communication Protocol Specifications for further details.

1) Set 01H for the “Use FPGA Enable” (Device code: 20H, command: 19H).

c. JTAG

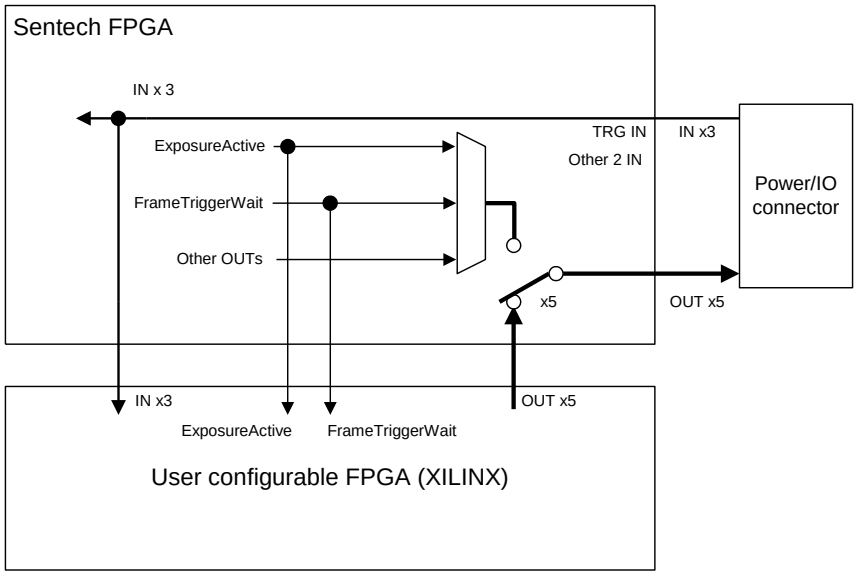
1) This JTAG connection is provided for the debugging procedures of the “User Configurable FPGA” program. The JTAG connector is connected to the “User Configurable FPGA”.
Notes:

- The rear panel of the camera masks the JTAG connector. The rear panel kit is available from Sentech for JTAG accessibility.
- Please see the “User configurable FPGA (XILINX) JTAG accessing instructions” for more detailed information.

d. User I/Os

The camera provides a total of eight I/O points. Three are designated as inputs and five are outputs. Each I/O point can be assigned (or connected) to any point in the “Sentech FPGA” or “User Configurable FPGA”. Please see the table under section III-C “Connection Information between devices” and section II “I/O Circuits” for more details.
Note: The input assignments in the Sentech FPGA are limited for the functions of “Exposure Out” and “Trigger Ready”.

1) Conceptual I/O Connection Diagram

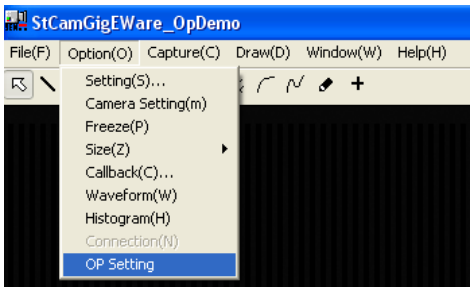


2) I/O Port Switching Method

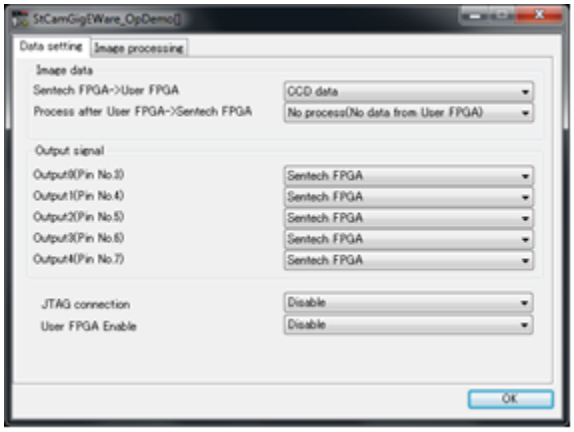
There are two different methods to achieve this switching:

a) By using the Sentech GUI “StCamGigEWare_OpDemo”
Also, please refer to “User Configurable FPGA (XILINX) Sample Codes.

1) Select “OP Setting” under “Option” in the menu.



2) Select which FPGA (Sentech FPGA or user configurable FPGA) sends the output signal to the 12pin power/IO connector at I/O Out0 to I/O Out4.



In the window above:
The Sentech FPGA sends the output signals to Output1 and 2 of the 12pin power/IO connector.
User configurable FPGA send output signals to Output 3, 4 and 5 of the 12pin power/IO connector.

b) Second Method: By changing the register value through the UART
Also, please refer to section “VI. The Communication Protocol Specifications” for more information.

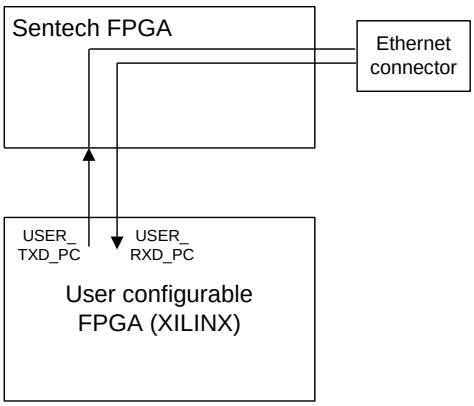
1) Set the output signal selection (Device code: 20H, command: C1H).
Select the output signal from the Sentech FPGA or the user configurable FPGA for each output.

2) Set the signals of the Power/IO connector (Device code: 00H, command: F0H, F8H and F9H).
Select the output signal from the Sentech FPGA when selecting the output signal from the Sentech FPGA.

e. UART through the Ethernet connector
The camera provides a serial communication channel (UART1) through the Ethernet connector for the user configurable FPGA. Through this communication channel, the user can change the register values in the “User configurable FPGA”.

1) Change the UART port from UART0 to UART1.
2) Setup the UART port as follows:

Baud Rate: 115,200 bps
Data Bit: 8bit
Parity: None
Stop Bit: 1bit
Flow Control: None

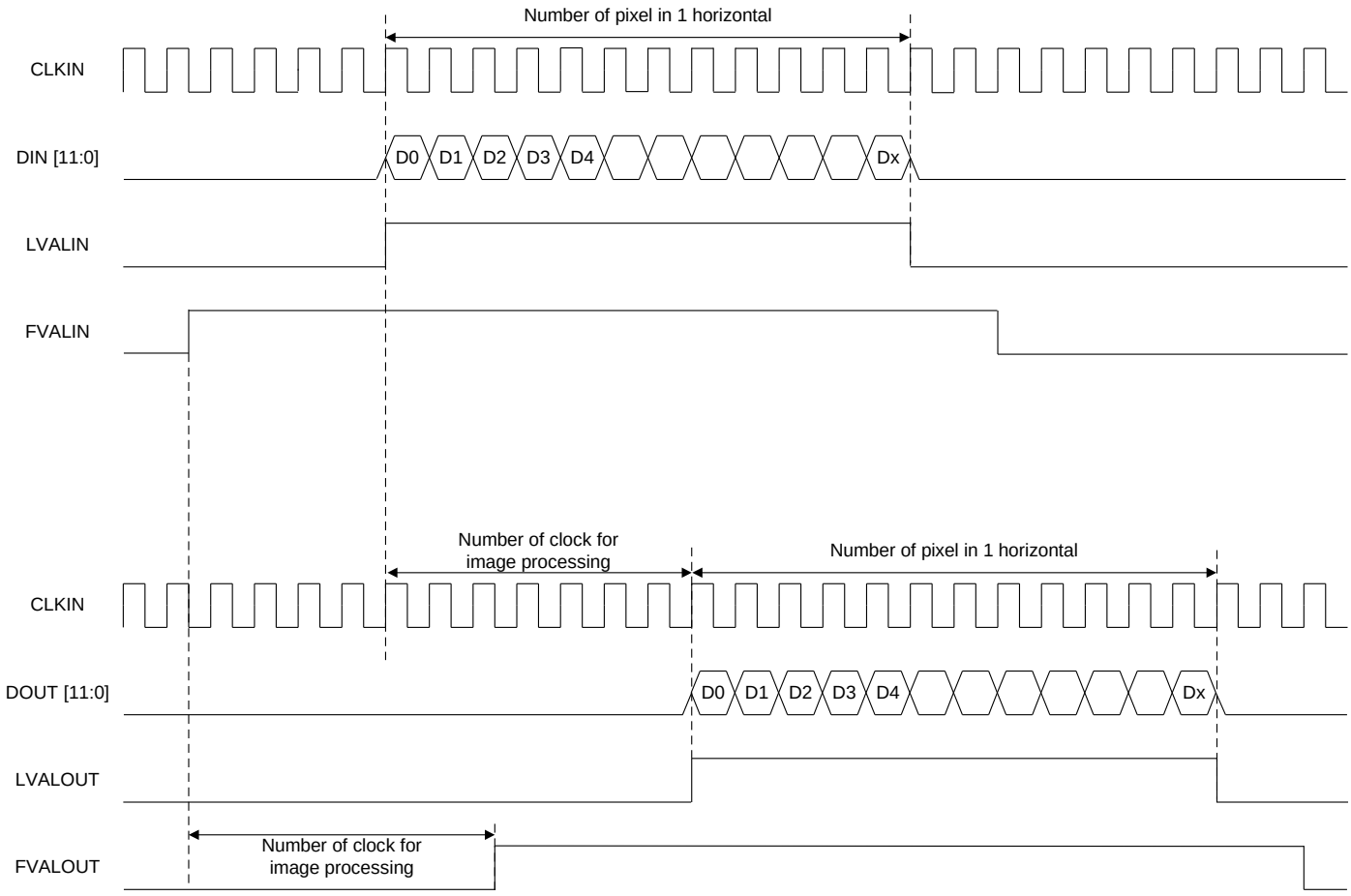


3. Important Design Consideration of the Data Timing and Handling
In the design process of the video processing program, please follow the conditions of the data timing below:

   a. DIN (image data), LVALIN and FVALIN are activated at the rising edge of CLKIN as the data comes into the user FPGA.

   b. As the data is sent back to the Sentech FPGA, add the delay equivalent to the process time in the user FPGA on LVALIN and FVALIN.

   c. As the data is sent back to the Sentech FPGA, DIN (image data), LVALIN and FVALIN must be activated at the rising edge of CLKIN.



D. Connection Information Between the Devices
It is not necessary to consider these data pin assignments if the pin assignment and the timing constraint files (Power_plus_000.ucf) are being used.

1. Connection between the user configurable FPGA (XILINX) and the Sentech FPGA

No	Signal Name	Direction	Discription	Pin No. of User FPGA
1	DIN0	input	Image Data bit0	B6
2	DIN1	input	Image Data bit1	A6
3	DIN2	input	Image Data bit2	A7
4	DIN3	input	Image Data bit3	A5
5	DIN4	input	Image Data bit4	B3
6	DIN5	input	Image Data bit5	B4
7	DIN6	input	Image Data bit6	A3
8	DIN7	input	Image Data bit7	A4
9	DIN8	input	Image Data bit8	A8
10	DIN9	input	Image Data bit9	B11
11	DIN10	input	Image Data bit10	B8
12	DIN11	input	Image Data bit11	A11
13	FVALIN	input	FVAL	C13
14	LVALIN	input	LVAL	C15
15	DOUT0	output	Image Data bit0	B13
16	DOUT1	output	Image Data bit1	B15
17	DOUT2	output	Image Data bit2	A16
18	DOUT3	output	Image Data bit3	A9
19	DOUT4	output	Image Data bit4	A17
20	DOUT5	output	Image Data bit5	B9
21	DOUT6	output	Image Data bit6	C4
22	DOUT7	output	Image Data bit7	C6
23	DOUT8	output	Image Data bit8	C7
24	DOUT9	output	Image Data bit9	C8
25	DOUT10	output	Image Data bit10	C9
26	DOUT11	output	Image Data bit11	C12
27	FVALOUT	output	FVAL	A13
28	LVALOUT	output	LVAL	A14
29	CLKIN	input	CLK	F11
30	SYS_RST_N	input	SYSTEM_RESET	AA12
31	USER_TXD_PC	input	UART_TX	E22
32	USER_RXD_PC	output	UART_RX	G22
34	USER_OUT_AUX0	output	USER_I/O	P22
35	USER_OUT_AUX1	output	USER_I/O	R22
36	USER_OUT_AUX2	output	USER_I/O	R20
37	USER_OUT_AUX3	output	USER_I/O	U22
38	USER_OUT_AUX4	output	USER_I/O	V20
39	USER_IN_AUX0	input	USER_I/O	W22
40	USER_IN_AUX1	input	USER_I/O	Y22
41	USER_IN_AUX2	input	USER_I/O	W19
42	ExposureActive	input	EXP_OUT	N17
43	FrameTriggerWait	input	TRG_RDY	N18
44	USER_TRG	output	TRG_OUT	D22

Note: Signal directions indicated as inputs and outputs are in reference to the user FPGA. “Input” refers to the signal from the Sentech FPGA to the user FPGA. “Output” refers to the signal from the user FPGA to the Sentech FPGA.

The image data transferred between the Sentech FPGA and the user FPGA is 12-bit data. The MSB (Most Significant Bit) is bit-11 and the LSB (Least Significant Bit) is bit-0. “DIN0-11” is the data from the Sentech FPGA to the user FPGA, and “COUT0-11” is the data from the user FPGA to the Sentech FPGA.

Please set Float, Pull-up or Pull-down for the unused input signal of the user configurable FPGA. Please set Pull-up or Pull-down, or set [H] or [L] with the RTL code, for the unused output signal of the user configurable FPGA.

2. Connection between the user configurable FPGA (XILINX) and DDR2

No	Signal Name	Direction	Discription	Pin No. of User FPGA
1	DDR_A0	output	Address0	G1
2	DDR_A1	output	Address1	K5
3	DDR_A2	output	Address2	K4
4	DDR_A3	output	Address3	L5
5	DDR_A4	output	Address4	K6
6	DDR_A5	output	Address5	K3
7	DDR_A6	output	Address6	K2
8	DDR_A7	output	Address7	M5
9	DDR_A8	output	Address8	L6
10	DDR_A9	output	Address9	V3
11	DDR_A10	output	Address10	V4
12	DDR_A11	output	Address11	W2
13	DDR_A12	output	Address12	W3
14	DDR_A13	-	Not use	F1
15	DDR_A14	-	Not use	F5
16	DDR_A15	-	Not use	F4
17	DDR_BA0	output	Bank address0	H5
18	DDR_BA1	output	Bank address1	H1
19	DDR_BA2	-	Not use	H2
20	DDR_D0	I/O	Data0	Y1
21	DDR_D1	I/O	Data1	W1
22	DDR_D2	I/O	Data2	R3
23	DDR_D3	I/O	Data3	T4
24	DDR_D4	I/O	Data4	T1
25	DDR_D5	I/O	Data5	R5
26	DDR_D6	I/O	Data6	T6
27	DDR_D7	I/O	Data7	T5
28	DDR_D8	I/O	Data8	P6
29	DDR_D9	I/O	Data9	P2
30	DDR_D10	I/O	Data10	P1
31	DDR_D11	I/O	Data11	N5
32	DDR_D12	I/O	Data12	L3
33	DDR_D13	I/O	Data13	M2
34	DDR_D14	I/O	Data14	K1
35	DDR_D15	I/O	Data15	L1
36	DDR_RAS#	output	Command inputs	F4
37	DDR_CAS#	output	Command inputs	G5
38	DDR_WE#	input	Command inputs	G6
39	DDR_CKE	output	Clock enable	H6
40	DDR_CK	output	Clock	U4
41	DDR_CK#	output	Clock	U5
42	DDR_LDQS	I/O	Data strobe for lower byte	U2
43	DDR_LDQS#	I/O	Data strobe for lower byte	V1
44	DDR_UDQS	I/O	Data strobe for upper byte	M6
45	DDR_UDQS#	I/O	Data strobe for upper byte	N7
46	DDR_ODT	output	On-die termination	F2
47	DDR_LDM	output	Input data mask for lower byte	U1
48	DDR_UDM	output	Input data mask for upper byte	R6

Note: The signal directions indicated as inputs and outputs are referencing the user FPGA. “Input” refers to a signal from the DDR2 to the user EEPROM and “Output” means from the user FPGA to EEPROM.

Please set Float, Pull-up or Pull-down for the unused input signal of the user configurable FPGA. Please set Pull-up or Pull-sown, or set [H] or [L] with the RTL code, for the unused output signal of the user configurable FPGA.

3. Connection between the user configurable FPGA (XILINX) and the EEPROM

No	Signal Name	Direction	Discription	Pin No. of User FPGA
1	ROM_512KBIT_CLK	output	Serial Clock for ROM	U20
2	ROM_512KBIT_nS	output	Chip Select for ROM	T17
3	ROM_512KBIT_DATA	output	Serial Data input for ROM	T20
4	ROM_512KBIT_Q	input	Serial Data output for ROM	T18
5	ROM_512KBIT_nW	output	Write Protect for ROM	R19

Note: The signal directions indicated as input and output are referencing the user FPGA. “Input” refers to a signal from the DDR2 to the user EEPROM and “output” refers to the signal from the user FPGA to the EEPROM.

Please set Float, Pull-up or Pull-down for the unused input signal of the user configurable FPGA.
Please set Pull-up or Pull-down, or set [H] or [L] with the RTL code, for the unused output signal of the user configurable FGPA.

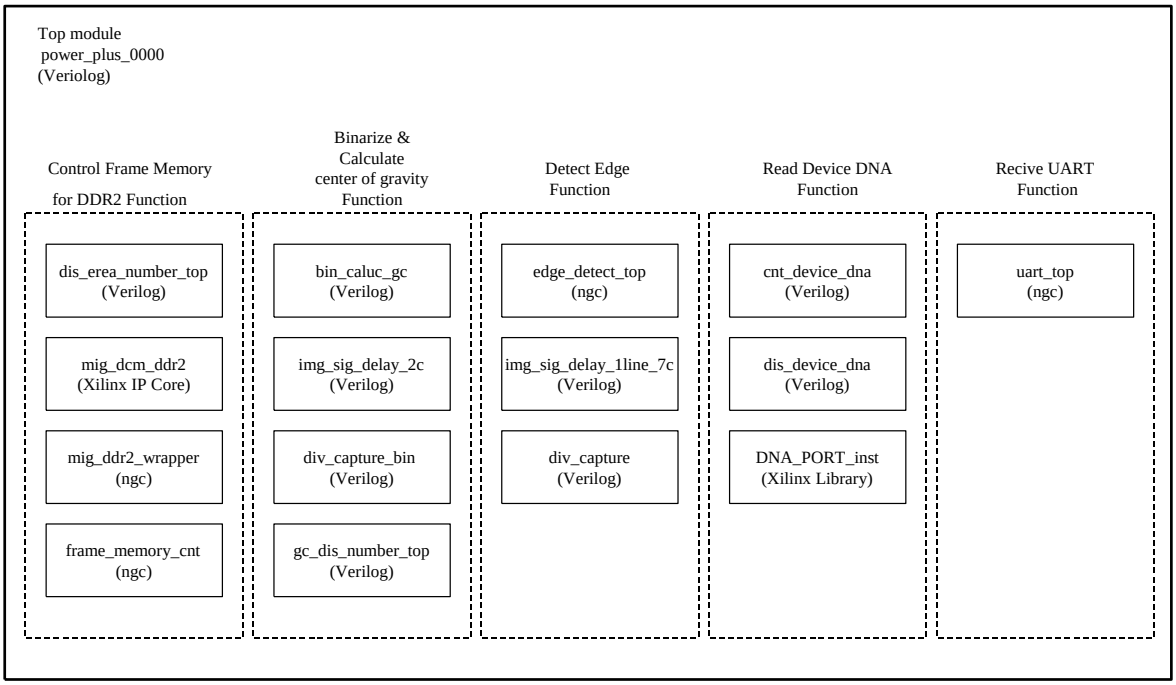
E. Development Guidelines

1. Module and Constraint Files

a. Top File
The top file is Power_plus.000.v file. The user should assign their codes onto this file.

b. Pin assignment and the Timing constraint file
The pin assignment and the timing constraint file is Power_plus.000.ucf file.
The user must add all constraints of their design onto this constraint file.

c. Structure of the Sample Code



2. Important Design Cautions
As you design the program in the user FPGA, it is imperative to synchronize all processes to the clock pulse rising edges given from the FPGA's pin number F11 (symbol CLKIN). Follow the four important notices listed below along with the Conceptual drawing of the FPGA programming.

Cautions:
1. Latch all signal timings of the image data, LVAL and FVAL coming from the Sentech FPGA at the rising edges of the clock pulse (symbol CLKIN).

2. In the same manner, the signal timings of the image data, LVAL and FVAL after the image processing must be latched at the rising edge of the clock pulse (symbol CLKIN).

3. When a selector is used in the process as shown as an example in the drawing, the signal timings of the image data, LVAL and FVAL must be latched at the rising edges of the clock pulse (symbol CLKIN).

4. The image data, LVAL and FVAL must be latched at the rising edges of the clock pulse (symbol CLKIN) prior to sending them back to the Sentech FPGA.

3. Notice for DDR2 Memory Usage

The DDR2 memory control IP core for the sample code was made by MIG3.3 (Core Generator) with the following settings:

Setting Item	Setting Value
Burst Length	4
Burst Type	Sequential
Output Driver Strength	Fullstrength
RTT(nominal)-ODT	75Ohm
DQS# Enable	Enable
USE DCM	check
Class for Address and Control	Class II
Class for Data	Class II
Debug Signal for Memory Controller	Disable
System Clock	Signal-Ended

The generated file
(\ipcore_dir\mig_dcm_ddr2\mig_dcm_ddr2\user_design\par\mig_dcm_ddr2_infrastructure_tip.v) was changed as follows:

105 line of mig_dcm_ddr2_infrastructure_top.v

```
/*
  generate
  if(`CLK_TYPE == "DIFFERENTIAL") begin : DIFF_ENDED_CLKS_INST

    IBUFGDS_LVDS_25  SYS_CLK_INST
     (
      .I  (sys_clk),
      .IB (sys_clkb),
      .O  (sys_clk_ibuf)
      );
  end else if(`CLK_TYPE == "SINGLE_ENDED") begin : SINGLE_ENDED_CLKS_INST

    IBUFG  SYS_CLK_INST
     (
      .I  (sys_clk_in),
      .O  (sys_clk_ibuf)
      );
  end
  endgenerate
*/

// CHANGE BY SENSOR TECHNOLOGY
  assign sys_clk_ibuf = sys_clk_in;
```

The timing constraint file, which is made by the IP core belongs to the ISE
(\ipcore_dir\mig_dcm_ddr2\mig_dcm_ddr2\user_design\par\mig_dcm_ddr2.ucf) is reflect to the Power_plus_000.ucf file.

To use the DDR2 memory, the optional setting of the ISE was changed to the following from the default setting

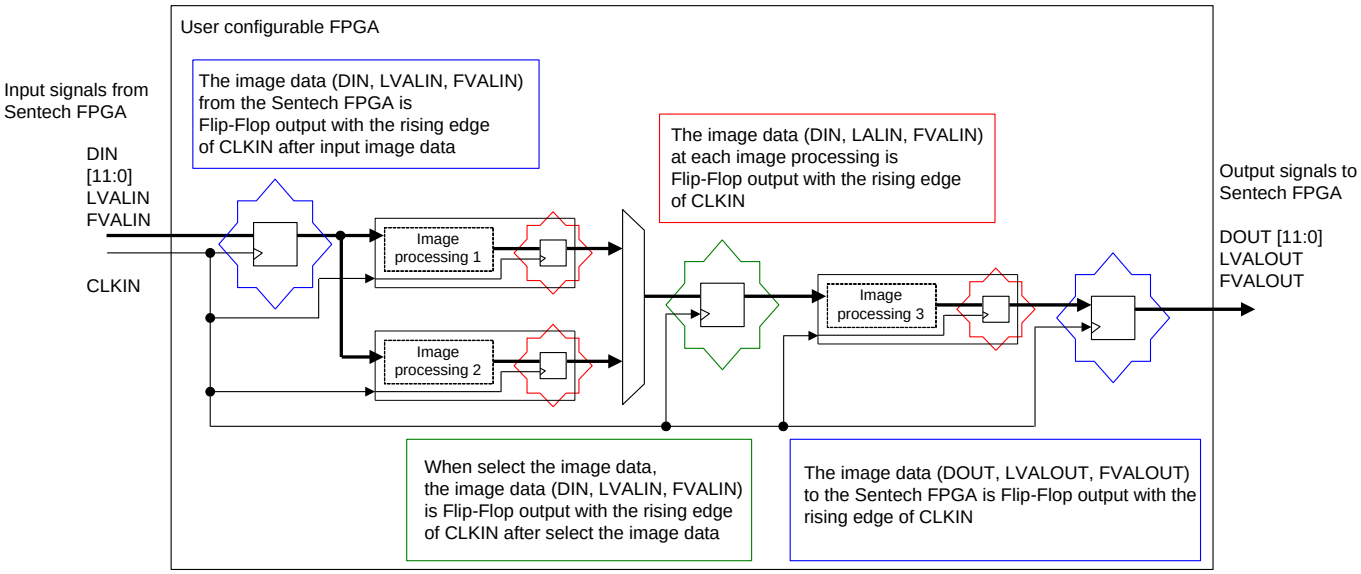
Category	Property name	Value
Synthesis Options	Keep Hierarchy	Soft

4. Recommendations for the image data handle between the Sentech FPGA and the User Configurable FPGA

   It is recommended to make the image processing synchronize with CLKIN when the image processing is in the user configurable FPGA.

   It is also recommended to set the timing restriction for securing the timing margin of CLKIN and the image data (DIN, DOUT, LVALIN, LVALOUT, FVALIN, FVALOUT) between the Sentech FPGA and the user configurable FPGA.

   Please check the sample code for details.



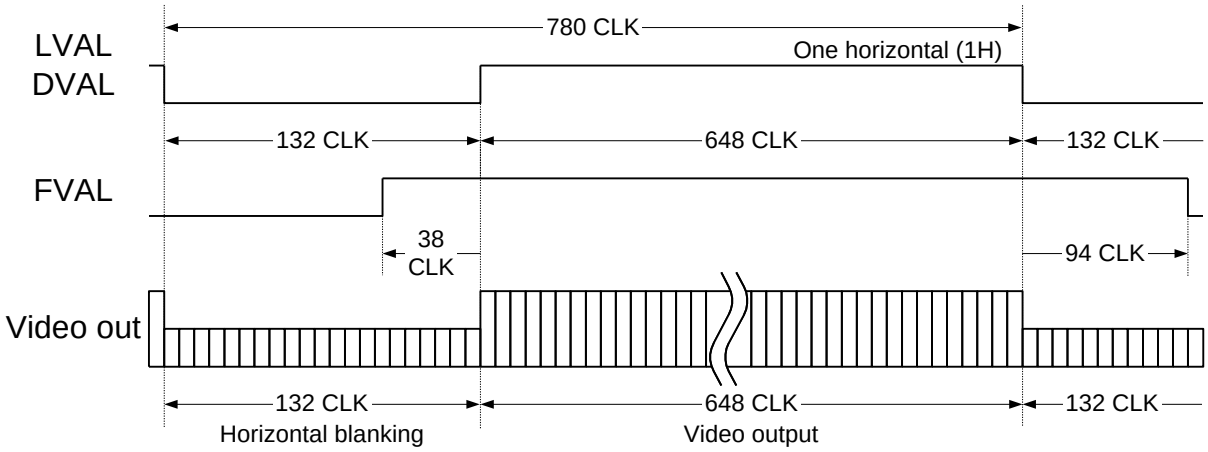
5. Copy Guard Function
   The user configurable FPGA (XILINX: XC3SD1800A) supports the “Device DNA security function” for FPGA design protection.
   The user configurable FPGA has a 57bit unique ID. This ID can be used as a security key.
   Please refer to the XILINX application note: WP266 for further details.

6. Schematics of the User Configurable FPGA (XILINX)
   Please refer to the “Schematics of user configurable FPGA (XILINX).

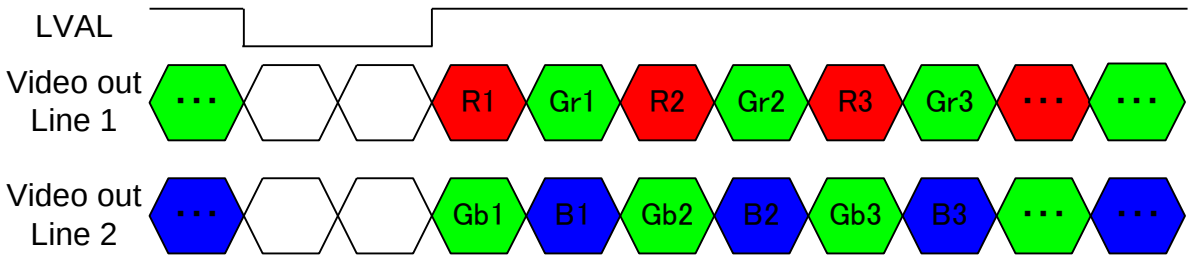
IV. The Camera Output Timing Charts

A. Horizontal Timing

1 CLK = 27.1605 nseconds



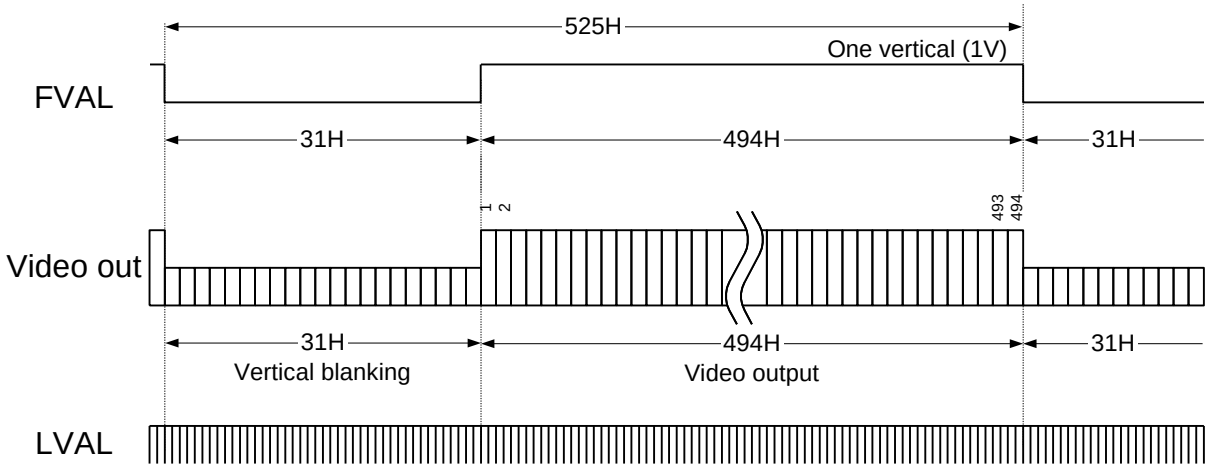
1. Color Bayer Order (This information is only for the STC-GEC33OX)



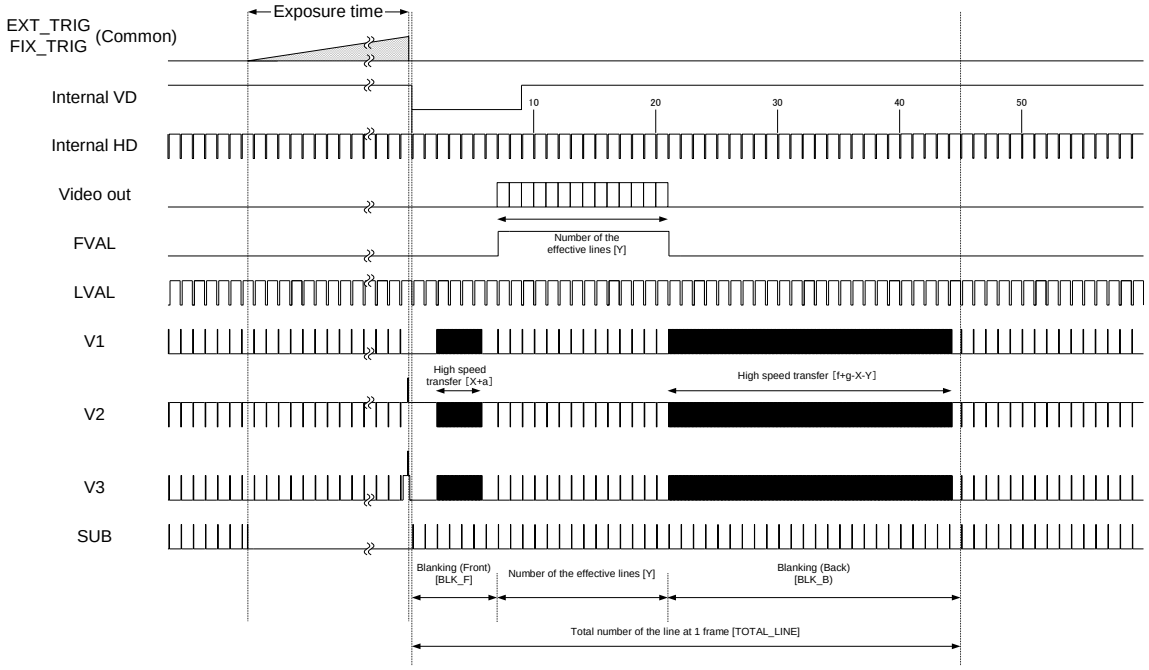
B. Vertical Timing

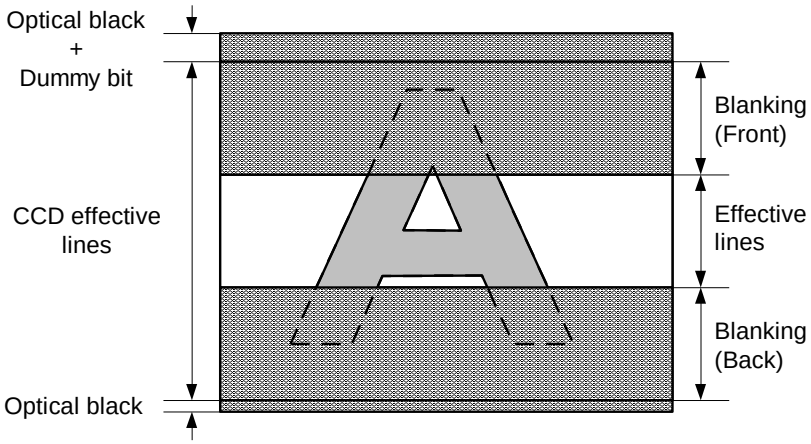
1 H = 21.1852 µseconds, 89.910172 Hz

1. Full Scanning



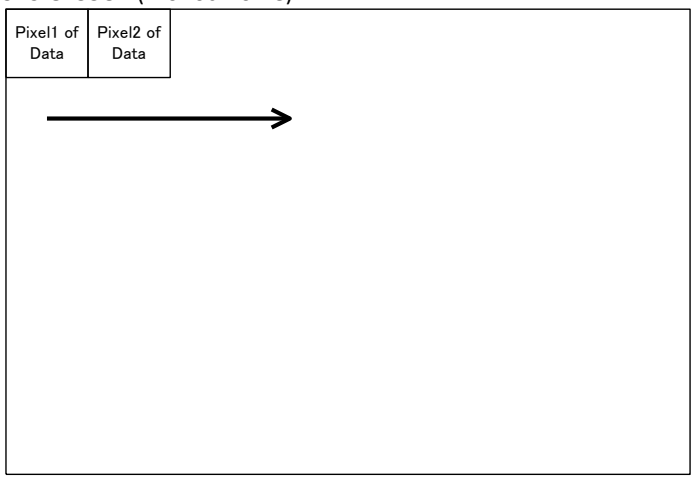
2. AOI


Exposure time
EXT_TRIG
FIX_TRIG (Common)
Internal VD
10
20
30
40
50
Internal HD
Video out
FVAL
Number of the
effective lines [Y]
LVAL
V1
High speed
transfer [X+a]
High speed transfer [f+g-X-Y]
V2
V3
SUB
Blanking (Front)
[BLK_F]
Number of the effective lines [Y]
Blanking (Back)
[BLK_B]
Total number of the line at 1 frame [TOTAL_LINE]


Optical black
+
Dummy bit
CCD effective
lines
Optical black
Blanking
(Front)
Effective
lines
Blanking
(Back)

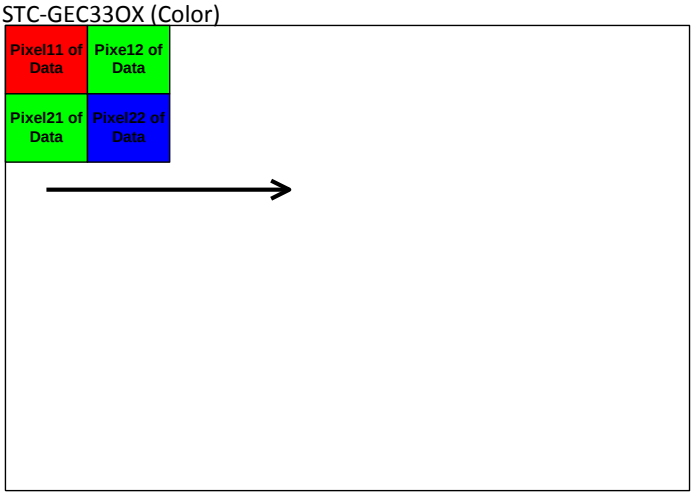
C. Transferring Image

STC-GE33OX (Monochrome)



Pixeln of Data: The transferring pixel
n: The order number

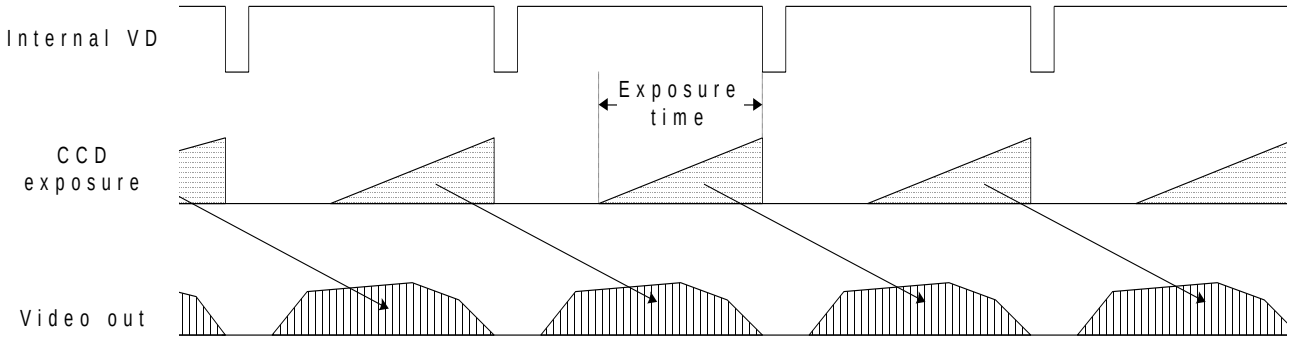
STC-GEC33OX (Color)



Pixelmn of Data: The transferring pixel
m: The line number
n: The order number

V. Camera Function Modes

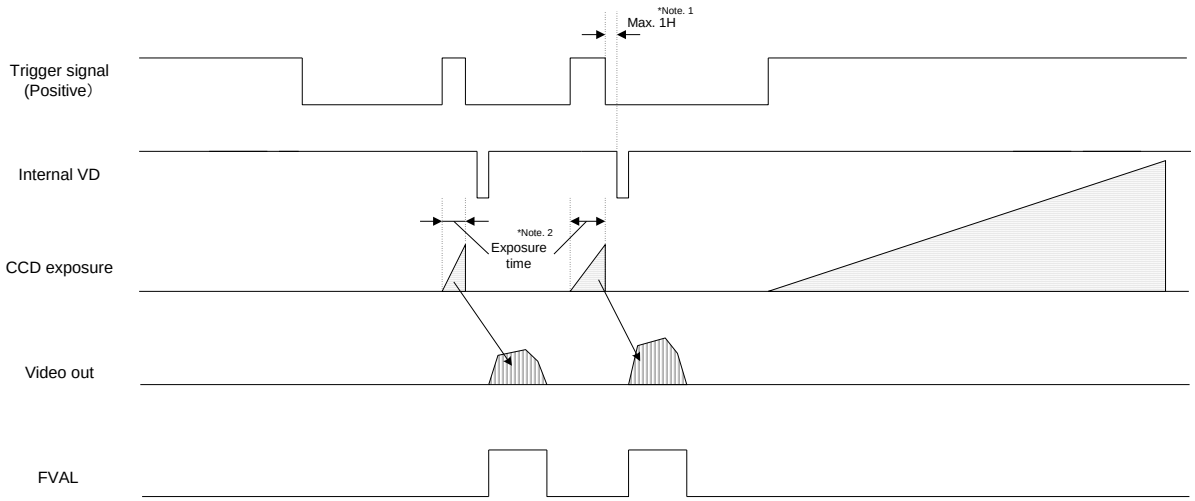
A. Normal Mode



B. Pulse Width Trigger Mode

In this trigger mode with positive polarity, the camera exposure starts at the rising edge of the trigger pulse and stops at the falling edge of the trigger pulse. Therefore, if positive polarity is selected, the exposure periods are the high states of the trigger pulse.

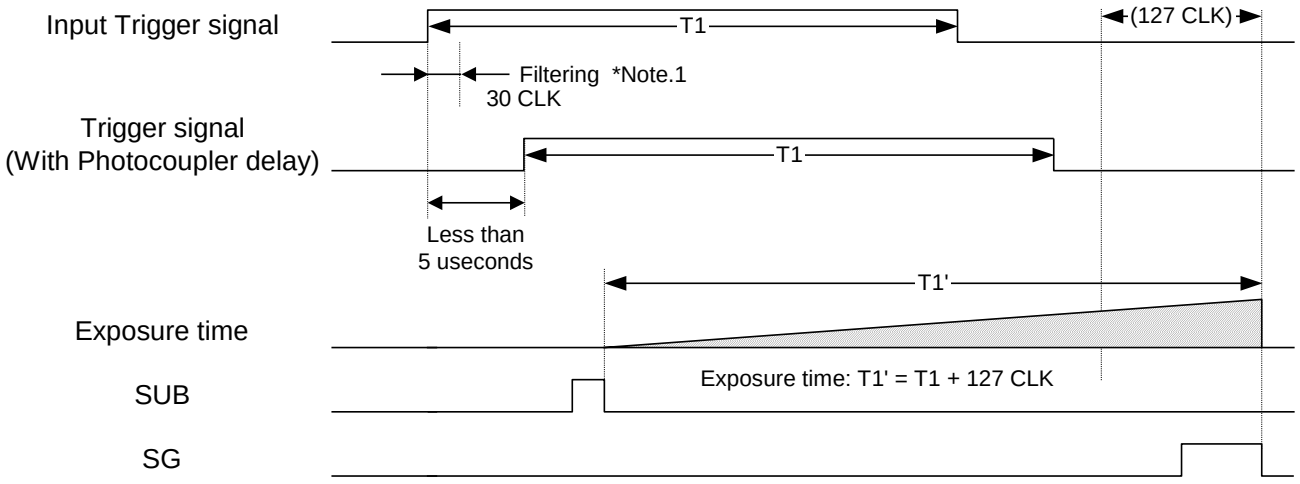
1. Timing



Notes:

- The video output is going to be V reset by the next internal HD signal immediately after the exposure is finished.
- The exposure time is set by the pulse width of the trigger signal.

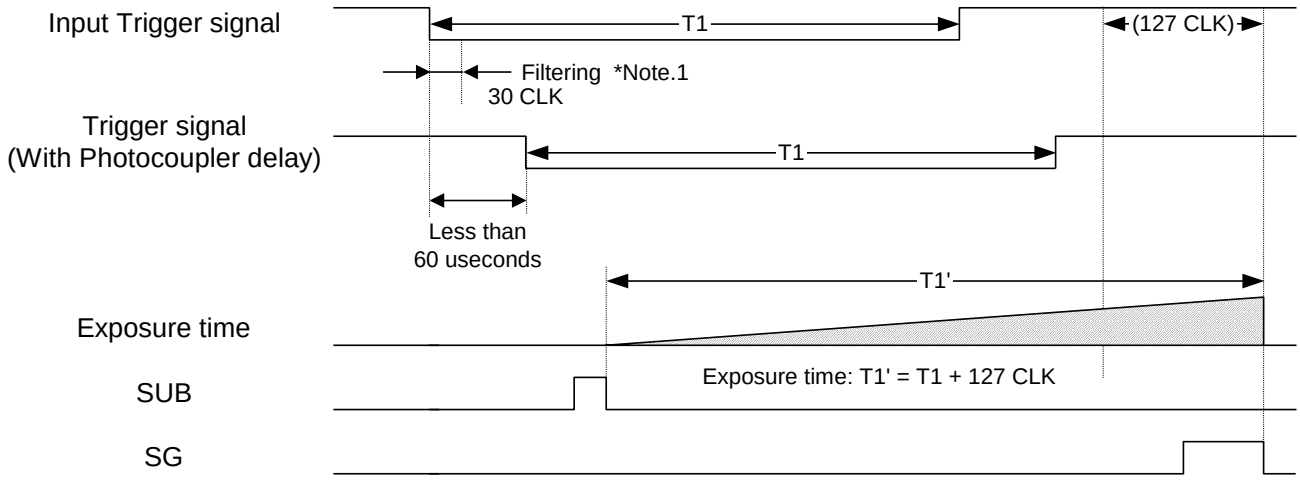
2. Exposure Timing with the Positive Polarity Trigger Signal



Notes:

- The trigger signal is removed by the filtering if the pulse width of the input trigger signal is less than 30 CLK. Please input a trigger signal with more than a 31 CLK pulse width
- The exposure will start 75 CLK after the rising edge of the trigger signal.

3. Exposure Timing with the Negative Polarity Trigger Signal



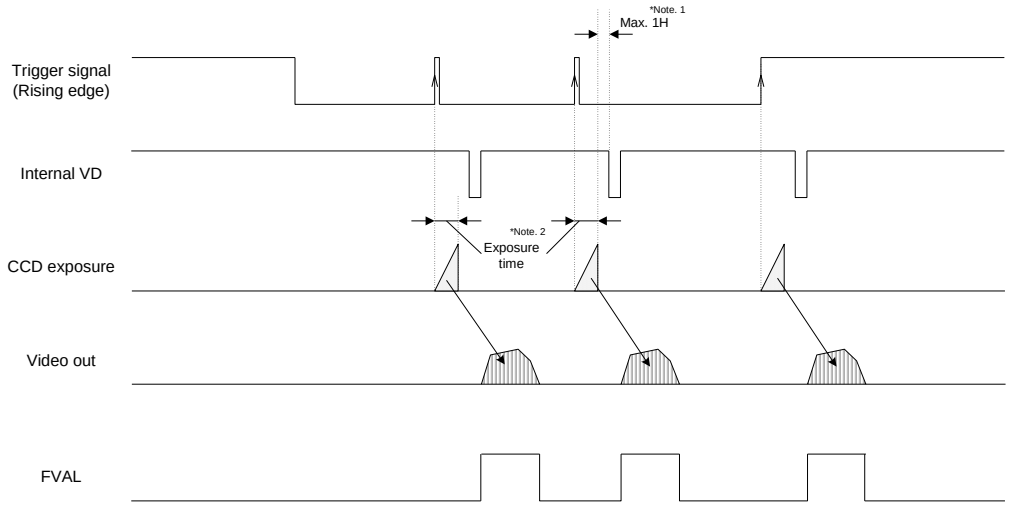
Notes:

- The trigger signal is removed by the filtering if the pulse width of the input trigger signal is less than 30 CLK. Please input a trigger signal with more than a 31 CLK pulse width
- The exposure will start 75 CLK after the rising edge of the trigger signal.

C. Edge Preset Trigger Mode

In this trigger mode, the camera exposure starts at the rising edge of the trigger pulse. The exposure duration time is preset by the DIP Switch settings.

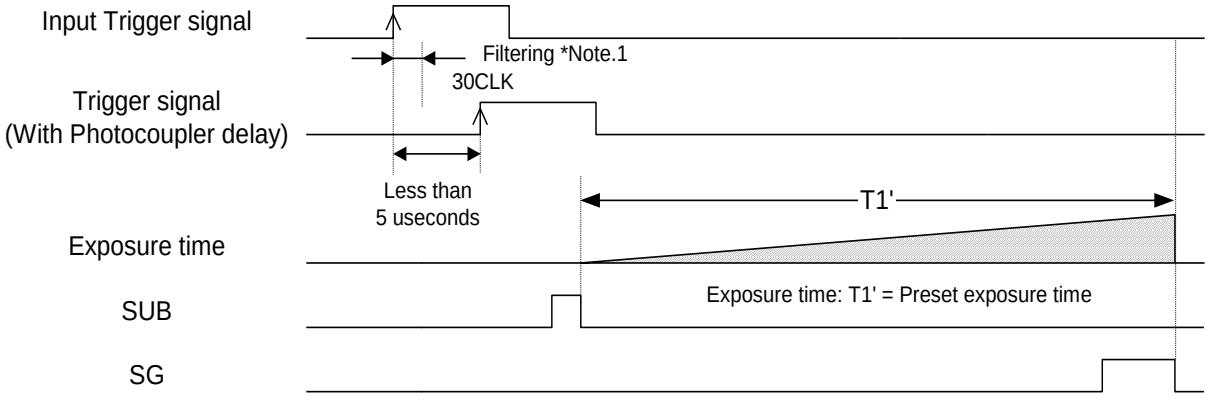
1. Timing



Notes:

- The video output is going to be V reset by the next internal HD signal immediately after the exposure is finished.
- The exposure time is set by the preset electronic shutter speed.

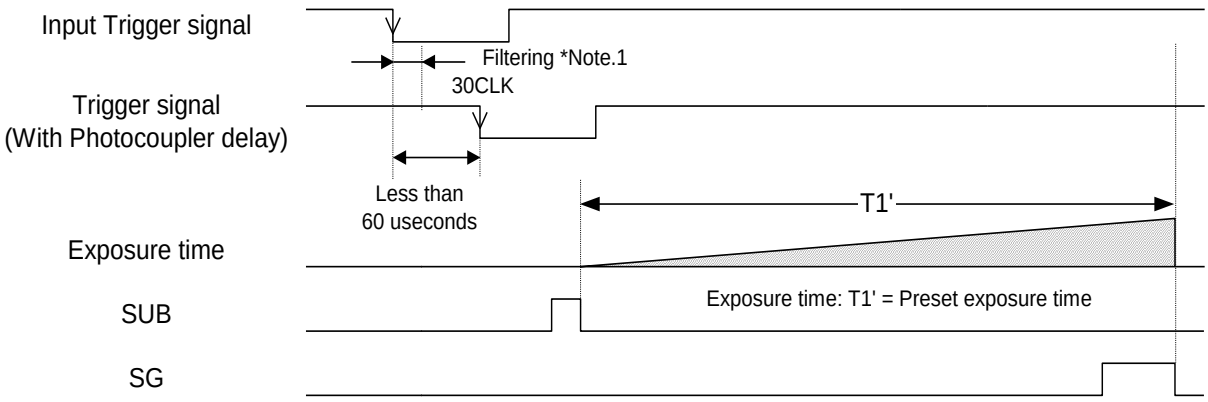
2. Exposure Timing with the Positive Polarity Trigger Signal



Notes:

- The trigger signal is removed by the filtering if the pulse width of the input trigger signal is less than 30 CLK. Please input a trigger signal with more than a 31 CLK pulse width
- The exposure will start 75 CLK after the rising edge of the trigger signal.

3. Exposure Timing with the Negative Polarity Trigger Signal



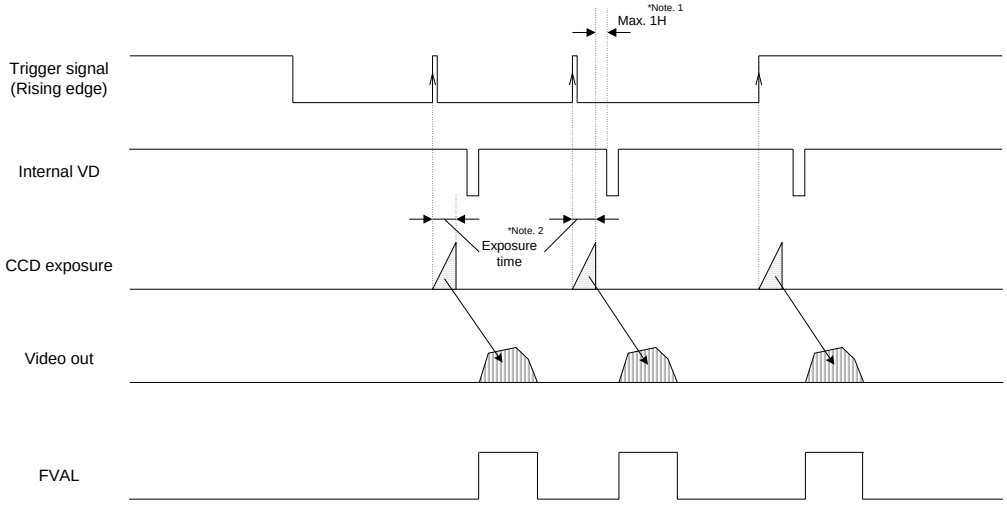
Notes:

- The trigger signal is removed by the filtering if the pulse width of the input trigger signal is less than 30 CLK. Please input a trigger signal with more than a 31 CLK pulse width
- The exposure will start 75 CLK after the rising edge of the trigger signal.

D. Edge Preset Trigger Mode (The trigger input while the image is out)
In this trigger mode, the camera exposure starts at the rising edge of the trigger pulse. The exposure duration time is preset by the DIP Switch settings.

It is necessary to disable the trigger signal mask with the communication when the trigger signal input is required while the image is out.
It is necessary to set the “H reset” at the exposure start mode to keep from generating additional noise on the image.

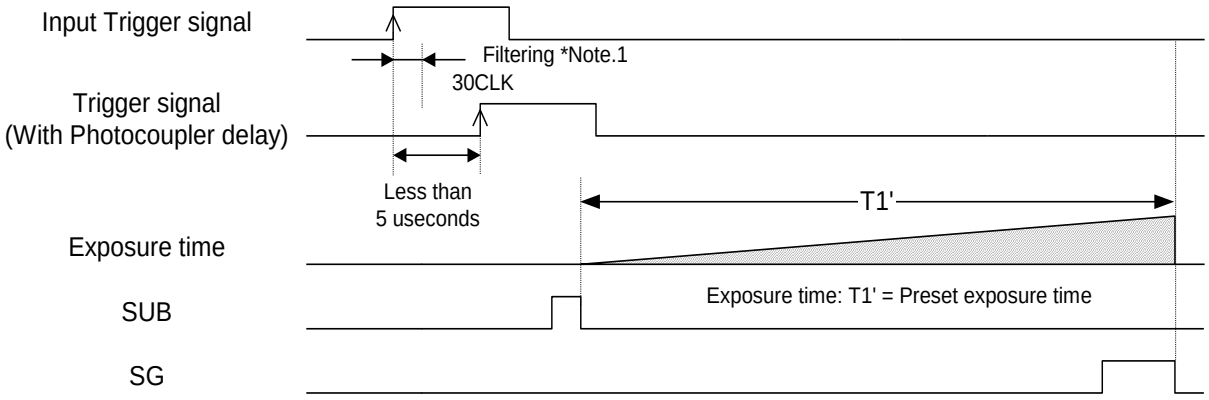
1. Timing



Notes:

- The video output is going to be V reset by the next internal HD signal immediately after the exposure is finished.
- The exposure time is set by the preset electronic shutter speed.

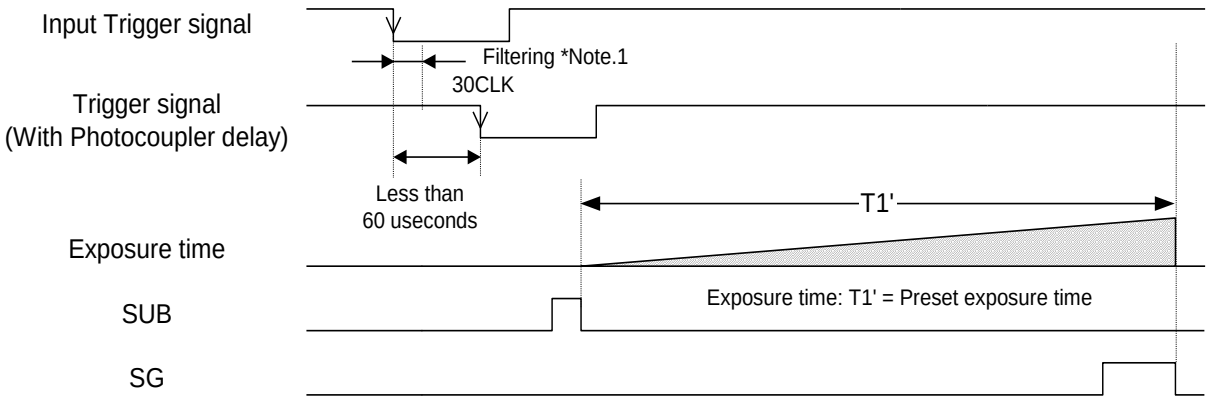
2. Exposure Timing with the Positive Polarity Trigger Signal



Notes:

- The trigger signal is removed by the filtering if the pulse width of the input trigger signal is less than 30 CLK. Please input a trigger signal with more than a 31 CLK pulse width
- The exposure will start 75 CLK after the rising edge of the trigger signal.

3. Exposure Timing with the Negative Polarity Trigger Signal



Notes:

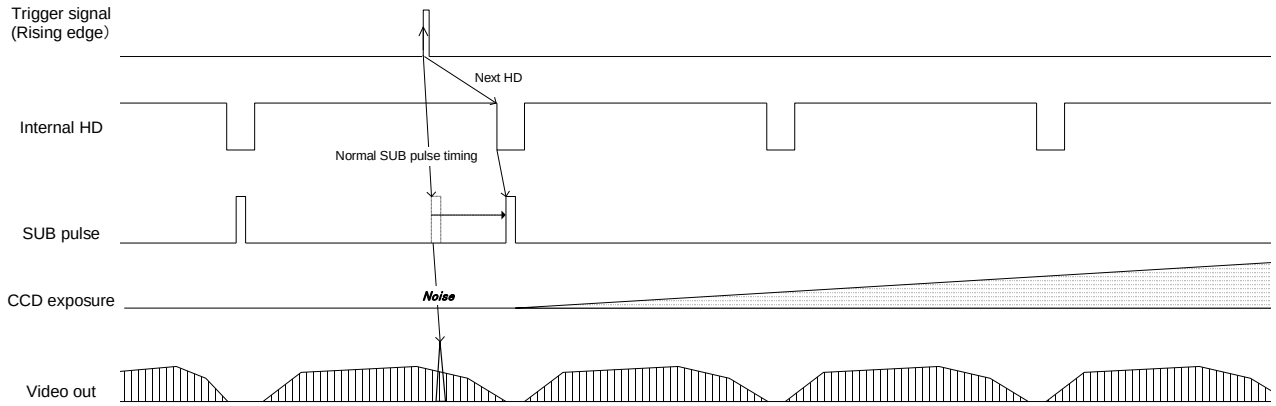
- The trigger signal is removed by the filtering if the pulse width of the input trigger signal is less than 30 CLK. Please input a trigger signal with more than a 31 CLK pulse width
- The exposure will start 75 CLK after the rising edge of the trigger signal.

E. H Reset Mode

In this mode, the exposure can be initiated during the video out from the camera without any horizontal noise. A SUB pulse is generated to sweep the charges during the horizontal blanking period to prevent from getting horizontal noises.

The image will have horizontal noise that is caused by generating the SUB pulse during the video out during normal mode (H Reset Mode is OFF)

The maximum delay to start the exposure from the trigger input is 1H.



VI. The Communication Protocol Specifications

This camera has a communication function that enables external devices (such as a PC) to control the camera functions. Please use the StCamGigEWare or StGigECtrl communication software or use the following communication protocol to communicate to the camera.

A. The Communication Method
UART (RS232C), Binary Communication

B. The Communication Settings

	Settings
Baud rate	115,200bps
Data bit	8bit
Parity	None
Stop bit	1bit
Flow control	None

C. The Communication Format

1. The format for sending data from the PC to the camera is as follows:

a. Sending the read command

SOF (8bit)	Device code (6bit)	Read (1bit)	Page selection (1bit)	Command code (8bit)	Data length (8bit)	Data (Dummy, 1byte)	EOF (8bit)

b. Sending the write command

SOF (8bit)	Device code (6bit)	Write (1bit)	Page selection (1bit)	Command code (8bit)	Data length (8bit)	Data (Data length byte)	EOF (8bit)

2. The format for receiving data form the camera is as follows:

a. After sending the read command

SOF (8bit)	Data length (8bit)	Data (Data length byte)	EOF (8bit)

b. After sending the write command

SOF (8bit)	Data length (8bit) "00"	Receiving code (8bit)	EOF (8bit)

3. Descriptions of the Format

Name	Descriptions
SOF	**S**tart **o**f the **f**rame Sets (or gets) the value is as “02H” always.
Device code	Sets "000000" when access to the camera function setting. Sets "100000" when access to the camera extend function setting. Please check the "The camera commands list" and "Description of the camera control commands"
Read / Write	Sets (or gets) “0” when send read command. Sets (or gets) “1” when send write command.
Page selection	Sets “0” when access to the command register of the camera Gets current data from the command register when sent read command. The data of the command register is replaced by the sent data when sent write command. **The data of the EEPROM is not replaced.** Sets “1” when access to the EEPROM of the camera The camera works with the data of the EEPROM when the power on the camera. Gets the data from the EEPROM when sent read. The data of the EEPROM is replaced by sent data when sent write command. The camera sends the receiving coce as "01H" to the PC after the data of the EEPROM is replaced.
Command code	**Please check from the following page.**
Data length	Data length (Unit: byte) Receiving data The data length is depending on the command after sent read command. The data length is “00H” after sent write command. Sending data The data length is 1 byte when send read command. The data length is depending on the command when send write command.
Data	The value of the data is depending on the command
EOF	**E**nd **o**f the **f**rame Sets (or gets) the value is as “03H” always
Receiving code	Result of the sending command

4. Command Example

Send the read command to read the 00H address data of the register

02, 00, 00, 01, 00, 03
SOF, (Device code/Read/Register), Command Code, Data Length, Data EOF

The return command
02, 01, 00, 03

D. The Camera Control Commands

1. The Camera Control Commands List

Notes:

- The data unit of each command is 1 byte (8bit)
- The data can be saved to the EEPROM if “x” is in the “Save to EEPROM” column in the list below.
- When the camera is powered on, it operates with the data of the EEPROM.

Device Code	Command No.	Read / Write	Save to EEPROM	Function	Initial data	Data range
000000	00 to 0FH			Reserved	-	-
	10H	Read / Write	x	The camera function mode 1 (8bit: D[7..0])	89H	
	11H	Read / Write	x	The camera function mode 2 (8bit: D[7..0])	0FH	
	12H	Read / Write	x	The camera function mode 3 (8bit: D[7..0])	00H	
	13H	Read / Write	x	The camera function mode 4 (8bit: D[7..0])	60H	
	14 to15H			Reserved	-	-
	16H	Read / Write	x	Software trigger mode (8bit: D[7..0])	00H	
	17H	Read / Write	x	Image data reset (8bit: D[7..0])	00H	
	18 to1FH			Reserved	-	-
	20H	Read / Write	x	The exposure time (useconds) of the electronic shutter (24bit: D[7..0])	0	0 to 16,777,215
	21H	Read / Write	x	The exposure time (useconds) of the electronic shutter (24bit: D[15..8])		
	22H	Read / Write	x	The exposure time (useconds) of the electronic shutter (24bit: D[24..16])		
	23 - 2FH			Reserved	-	-
	30H	Read / Write	x	CDS gin (8bit: D[7..0])	0	0 to 255
	31H	Read / Write	x	The digital gain (8bit: D[7..0])	The factory adjusted value	
	32H	Read / Write	x	The gain offset (8bit: D[7..0])	The factory adjusted value	
	33 to 37H			Reserved	-	-
	38H	Read / Write	x	The clamp level (8bit: D[7..0])	9	0 to 31
	39 to 3DH			Reserved	-	-
	3EH	Read / Write	x	White clip for the test pattern (16bit: D[15..8])	1,023	0 to 4,095
	3FH	Read / Write	x	White clip for the test pattern (16bit: D[7..0])		
	40 to 4FH			Reserved	-	-
	50H	Read / Write	x	The trigger delay time (useconds) (Integer) (24bit: D[7..0])	0	0 to 2,000,000
	51H	Read / Write	x	The trigger delay time (useconds) (Integer) (24bit: D[15..8])		
	52H	Read / Write	x	The trigger delay time (useconds) (Integer) (24bit: D[23..16])		
	53H	Read / Write	x	The trigger delay time (useconds) (Decimal) (8bit: D[7..0])		
	54 to 57H			Reserved	-	-
	58H	Read / Write	x	Frame rate (Hz) (Integer) (16bit: D[7..0])	89.91172	0.72028 to 360.33325
	59H	Read / Write	x	Frame rate (Hz) (Integer) (16bit: D[15..8])		
	5AH	Read / Write	x	Frame rate (Hz) (Decimal) (24bit: D[7..0])		
	5BH	Read / Write	x	Frame rate (Hz) (Decimal) (24bit: D[15..8])		
	5CH	Read / Write	x	Frame rate (Hz) (Decimal) (24bit: D[23..16])		
	5D to 77H			Reserved	-	-
	78H	Read / Write	x	Test pattern selection (8bit: D[7..0])	00H	
	79H	Read / Write	x	Image effect selection (8bit: D[7..0])	00H	
	7A to 7FH			Reserved	-	-
	80H	Read / Write		EEPROM control (8bit: D[7..0])	00H	
	81 to EFH			Reserved	-	-
	F0H	Read / Write	x	The signals of the power/IO connector (8bit: D[7..0])	20H	
	F1H	Read / Write	x	UserOutput signal for the power/IO connector (8bit: D[7..0])	00H	
	F2 to F7H			Reserved	-	-
	F8H	Read / Write	x	The signals of the power/IO connector (8bit: D[7..0])	00H	
	F9H	Read / Write	x	The signals of the power/IO connector (8bit: D[7..0])	00H	
	FA to FFH			Reserved	-	-

Device Code	Command No.	Read / Write	Save to EEPROM	Function	Initial data	Data range
100000	00 to 17H			Reserved	-	-
	18H	Read / Write	x	JTAG for User configurable FPGA (8bit: D[7..0])	00H	
	19H	Read / Write		User configurable FPGA Enable (8bit: D[7..0])	00H	
	1A to 1FH			Reserved	-	-
	20H	Read / Write	x	Exposure mode (8bit: D[7..0])	00H	
	21H	Read / Write	x	AGC maximum limit (8bit: D[7..0])	255	0 to 255
	22H			Reserved	-	-
	23H	Read / Write	x	The upper limit of the electronic shutter for auto shutter (20bit: D[7..0])	11,122	0 to 1,048,575
	24H	Read / Write	x	The upper limit of the electronic shutter for auto shutter (20bit: D[15..8])		
	25H	Read / Write	x	The upper limit of the electronic shutter for auto shutter (20bit: D[20..16])		
	26H	Read / Write	x	The lower limit of the electronic shutter for auto shutter (20bit: D[7..0])	0	0 to 1,048,575
	27H	Read / Write	x	The lower limit of the electronic shutter for auto shutter (20bit: D[15..8])		
	28H	Read / Write	x	The lower limit of the electronic shutter for auto shutter (20bit: D[20..16])		
	29H	Read / Write	x	Weight1 for ALC (8bit: D[7..0])	11H	D3 to D0: 0 to 15 D7 to D4: 0 to 15
	2AH	Read / Write	x	Weight2 for ALC (8bit: D[7..0])	11H	D3 to D0: 0 to 15 D7 to D4: 0 to 15
	2BH	Read / Write	x	Weight3 for ALC (8bit: D[7..0])	1AH	D3 to D0: 0 to 15 D7 to D4: 0 to 15
	2CH	Read / Write	x	Weight4 for ALC (8bit: D[7..0])	11H	D3 to D0: 0 to 15 D7 to D4: 0 to 15
	2DH	Read / Write	x	Weight5 for ALC (8bit: D[7..0])	01H	D3 to D0: 0 to 15 D7 to D4: 0
	2EH	Read / Write	x	Target brightness for ALC (8bit: D[7..0])	128	0 to 255
	2FH	Read / Write	x	ALC peak-average (8bit: D[7..0])	0	0 to 255
	30H	Read / Write	x	Vertical_1 position for the ALC weight area (16bit: D[7..0])	32	0 to 493
	31H	Read / Write	x	Vertical_1 position for the ALC weight area (16bit: D[15..8])		
	32H	Read / Write	x	Vertical_2 position for the ALC weight area (16bit: D[7..0])	196	0 to 493
	33H	Read / Write	x	Vertical_2 position for the ALC weight area (16bit: D[15..8])		
	34H	Read / Write	x	Vertical_3 position for the ALC weight area (16bit: D[7..0])	298	0 to 493
	35H	Read / Write	x	Vertical_3 position for the ALC weight area (16bit: D[15..8])		
	36H	Read / Write	x	Vertical_4 position for the ALC weight area (16bit: D[7..0])	462	0 to 493
	37H	Read / Write	x	Vertical_4 position for the ALC weight area (16bit: D[15..8])		
	38H	Read / Write	x	Horizontal_1 position for the ALC weight area (16bit: D[7..0])	36	0 to 647
	39H	Read / Write	x	Horizontal_1 position for the ALC weight area (16bit: D[15..8])		
	3AH	Read / Write	x	Horizontal_2 position for the ALC weight area (16bit: D[7..0])	252	0 to 647
	3BH	Read / Write	x	Horizontal_2 position for the ALC weight area (16bit: D[15..8])		
	3CH	Read / Write	x	Horizontal_3 position for the ALC weight area (16bit: D[7..0])	396	0 to 647
	3DH	Read / Write	x	Horizontal_3 position for the ALC weight area (16bit: D[15..8])		
	3EH	Read / Write	x	Horizontal_4 position for the ALC weight area (16bit: D[7..0])	612	0 to 647
	3FH	Read / Write	x	Horizontal_4 position for the ALC weight area (16bit: D[15..8])		
	40H	Read / Write	x	White balance mode (8bit: D[7..0])	00H	
	41H	Read / Write	x	Preset_1 white balance (Red gain) (8bit: D[7..0])	0	0 to 255
	42H	Read / Write	x	Preset_1 white balance (Gr gain) (8bit: D[7..0])	0	0 to 255
	43H	Read / Write	x	Preset_1 white balance (Blue gain) (8bit: D[7..0])	0	0 to 255
	44H	Read / Write	x	Preset_1 white balance (Gb gain) (8bit: D[7..0])	0	0 to 255
	45H	Read / Write	x	Preset_2 white balance (Red gain) (8bit: D[7..0])	0	0 to 255
	46H	Read / Write	x	Preset_2 white balance (Gr gain) (8bit: D[7..0])	0	0 to 255
	47H	Read / Write	x	Preset_2 white balance (Blue gain) (8bit: D[7..0])	0	0 to 255
	48H	Read / Write	x	Preset_2 white balance (Gb gain) (8bit: D[7..0])	0	0 to 255
	49H	Read / Write	x	Preset_3 white balance (Red gain) (8bit: D[7..0])	0	0 to 255
	4AH	Read / Write	x	Preset_3 white balance (Gr gain) (8bit: D[7..0])	0	0 to 255
	4BH	Read / Write	x	Preset_3 white balance (Blue gain) (8bit: D[7..0])	0	0 to 255
	4CH	Read / Write	x	Preset_3 white balance (Gb gain) (8bit: D[7..0])	0	0 to 255
	4DH			Reserved	-	-
	4EH	Read / Write	x	Threshold for auto white balance (16bit: D[7..0])	3,072	0 to 4,095
	4FH	Read / Write	x	Threshold for auto white balance (16bit: D[16..8])		

Device Code	Command No.	Read / Write	Save to EEPROM	Function	Initial data	Data range
100000	50H	Read / Write	x	Y_offset for AOI (8bit: D[7..0])	0	4 <= Y <= 494 Y: Y_offset + Height
	51H	Read / Write	x	Y_offset for AOI (16bit: D[15..8])		
	52H	Read / Write	x	Height for AOI (8bit: D[7..0])	494	4 <= Y <= 494 Y: Y_offset + Height
	53H	Read / Write	x	Height for AOI (16bit: D[15..8])		
	54H	Read / Write	x	X_offset for AOI (8bit: D[7..0])	0	8 <= X <= 648 X: X_offset + width
	55H	Read / Write	x	X_offset for AOI (16bit: D[15..8])		
	56H	Read / Write	x	Width for AOI (8bit: D[7..0])	648	8 <= X <= 648 X: X_offset + width
	57H	Read / Write	x	Width for AOI (16bit: D[15..8])		
	58H	Read / Write	x	Vertical_1 position for the white balance area (16bit: D[7..0])	0	0 to 493
	59H	Read / Write	x	Vertical_1 position for the white balance area (16bit: D[15..8])		
	5AH	Read / Write	x	Vertical_2 position for the white balance area (16bit: D[7..0])	493	0 to 493
	5BH	Read / Write	x	Vertical_2 position for the white balance area (16bit: D[15..8])		
	5CH	Read / Write	x	Horizontal_1 position for the white balance area (16bit: D[7..0])	0	0 to 647
	5DH	Read / Write	x	Horizontal_1 position for the white balance area (16bit: D[15..8])		
	5EH	Read / Write	x	Horizontal_2 position for the white balance area (16bit: D[7..0])	647	0 to 647
	5FH	Read / Write	x	Horizontal_2 position for the white balance area (16bit: D[15..8])		
	60H	Read / Write	x	Camera mode1 (8bit: D[7..0])	00H	
	61 to 7FH			Reserved	-	-
	80H	Read / Write	x	Push set white balance (Red gain) (8bit: D[7..0])	0	0 to 255
	81H	Read / Write	x	Push set white balance (Gr gain) (8bit: D[7..0])	0	0 to 255
	82H	Read / Write	x	Push set white balance (Blue gain) (8bit: D[7..0])	0	0 to 255
	83H	Read / Write	x	Push set white balance (Gb gain) (8bit: D[7..0])	0	0 to 255
	84 to 8FH			Reserved	-	-
	90H	Read / Write	x	Iris lens adjustment (8bit: D[7..0])	80	0 to 255
	91H			Reserved	-	-
	92H	Read / Write	x	Iris lens manual adjustment (8bit: D[7..0])	01H	
	93 to BFH			Reserved	-	-
	C0H	Read / Write	x	Image data between FPGAs (8bit: D[7..0])	00H	
	C1H	Read / Write	x	Output signal selection (8bit: D[7..0])	00H	
	C2 toFFH			Reserved	-	-

2. Description of the Camera Control Commands (Device Code: 000000)

Note: The underline settings are the factory default settings.

<table>
<tr><th>Command No.</th><th>Command Descriptions</th></tr>
<tr><td>10H:
MOD1[7..0]</td><td>[The camera function mode 1] Initial data: 89H
This sets the camera function mode.
D[7..0]
<table>
<tr><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td></tr>
</table>

D7: Continuous/Trigger Mode — 0: Auto — 1: Manual
D6: Trigger Polarity — 0: Positive — 1: Negative
D5: Trigger Mode — 0: Edge Preset — 1: Pulse width
D4: Binning Mode — 0: OFF (Normal) — 1: ON (Binning)
D3: Scanning Mode — 0: Full Scanning — 1: Partial Scanning
D2 to D0: No Function — Always set as “001”</td></tr>
<tr><td>11H:
MOD2[7..0]</td><td>[The camera function mode 2] Initial data: 0FH
This sets the camera function mode.
D[7..0]
<table>
<tr><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td></tr>
</table>

D7 to D6: No Function — Always set as “00”
D5: TG Reset — 0: TG Partial Reset — 1: TG Partial Reset OFF
D4: Smear Half Reduction — 0: OFF — 1: ON
D3: Function Mode — 0: Trigger Mode — 1: Continuous Mode
D2 to D0: No Function — Always set as “111”

Notes:
• The function mode is enabled when the “Continuous/Trigger mode (MOD1-D7)” is manual.
• There is no video output without the trigger signal input while the camera works with the trigger mode.</td></tr>
<tr><td>12H:
MOD3[7..0]</td><td>[The camera function mode 3] Initial data: 00H
Sets the camera function mode.
D[7..0]
<table>
<tr><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td></tr>
</table>

D7 to D6: Video Out — 00: 10bit
01: 8bit
10: 12bit
11: RGB 8bit
D5: Trigger Signal Type — 0: Software Trigger
1: Hardware Trigger (trigger signal input from 5pin of Power/IO connector)
D4 to D3: Exposure Start Mode — 00: Normal
1: ON (Binning)
10 to 11: H Reset
01: No function (Prohibited settings. Do not set these values)
D2 to D0: No Function — Always set as “000”</td></tr>
</table>

<table>
<tr><th>Command No.</th><th>Command Descriptions</th></tr>
<tr><td>13H:
MOD4[7..0]</td><td>[The camera function mode 4] Initial data: 60H
This sets the camera function mode.
D[7..0]
<table>
<tr><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td></tr>
</table>

D7: No Function — Always set as “0”
D6: Trigger signal mask while the image is out — 0: OFF 1: ON (Invalid trigger signal while the image is out)
D5 to D0: No Function — Always set as “100000”</td></tr>
<tr><td>16H:
SOFTRG[7..0]</td><td>[Software Trigger Setting] Initial data: 00H
This sets the source of the software trigger.
D[7..0]
<table>
<tr><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td></tr>
</table>

D7 to D6: Software Trigger Source Selection — 00: Programming Software Trigger
01: User configurable FPGA generates the trigger
10: Command Software Trigger
(200 unseconds pulse width trigger signal)
11: No Function
(Prohibited settings – do NOT set these values)
D5 to D1: No Function — Always set as “00000”
D0: Generate command software trigger — 0: Hold (Low State) 1: Generate command software trigger (200 unseconds high state)

Notes:
• The software trigger source selection is enabled when the “Trigger signal type (MOD3-D5)” is the software trigger (sets as 0).
• When using the “Programming software trigger”, please set up the pulse duration, the trigger signal interval and generate the trigger signal with the “StGigE SDK”.
• When using “User Configurable FPGA Generates Trigger”, please generate a trigger signal with more than a 200 unseconds pulse duration in the user configurable FPGA.
• When the “Command Software Trigger” is selected, it is necessary to generate the software trigger with the “Generate command software trigger (SOFTRIG-D0)”.</td></tr>
<tr><td>17H:
IMAGEREST
[7..0]</td><td>[Image data reset] Initial data: 00H
Reset the image data (FVAL, LVAL and the image data).
Change from the reset to the image data out after the start the image acquisition.
The image data is not output when the image data is reset.

D7 to D1: No Function — Always set as “000”
D0: Image data reset — 0: FVAL/LVAL/Image data reset (FVAL, LVAL and the image data are low state data
1: FVAL/LVAL/Image data out</td></tr>
<tr><td>20H: EXPTM
[7..0]
21H: EXPTM
[15..8]
22H: EXPTM
[23..16]</td><td>[The exposure time (useconds0 of the electronic shutter]
Initial data: EXPTM[23..0] = 0, data range: 0 to 16,777,215
Sets the exposure time for the electronic shutter.

Exposure time = EXPTM[23..0] useconds

When set as 0, the electronic shutter is OFF.</td></tr>
</table>

Command No.	Command Descriptions
30H: PGA[7..0]	[CDS gain] Initial data: PGA[7..0] = 0, data range: 0 to 255 Sets the CDS gain (programmable gain) CDS gain = 6.16 + 0.04 x (PGA[7..0] x 2 + GOFS[7..0]) dB *CDS_BASEGAIN[15..0]: The gain base offset (The value of the address 5EH and 5FH) *GOFS[7..0]: The gain offset (The value of the address 32H)
31H: DGB[7..0]	[The digital gain] Initial data: DGB[7..0] = The factory adjusted value Video level = (Input video level – CLAMP level) x (1+DGB[7..0] / 128) + CLAMP Level *CLAMP Level: Clamp level (The calculated value of the address 38H)
32H: GOFS[7..0]	[The gain offset] Initial data: GOFS[7..0] = The factory adjusted value, data range: 0 to 255
38H: CLAMP[7..0]	[The clamp level] Initial data: CLAMP[7..0] = 9, data range: 0 to 31 This sets the clamp level (The clamp level of the black signal). Clamp level = CLAMP[7..0] x 8 + 56 (for 12 bit output) Clamp level = (CLAMP[7..0] x 8 + 56) / 4 (for 10 bit output) Clamp level = (CLAMP[7..0] x 8 + 56) / 16 (for 8 bit output) Whenever a value greater than 31 is set, it will automatically set to 31
3EH: WHITE_CLIP[15..8] 3FH: WHITE_CLIP[7..0]	[The white clip level for the white clip test pattern] Initial data: WHITE_CLIP[15..0] = 1023, data range: 0 to 4095 Sets the white clip level for the white clip test pattern
50H: DELAY_I[7..0] 51H: DELAY_I[15..8] 52H: DELAY_I[23..16]	[The delay time (usecond, integer) for the trigger signal] Initial data: DELAY_I[23..0] = 0, data range: 0 to 2,000,000 This sets the delay time (as usecond) that is from the trigger signal input to the start of the exposure. Delay time for the trigger signal = (DELAY_I[23..0]). (DELAY_F[7..0] useconds
53H: DELAY_F[7..0]	[The delay time (usecond, decimal) for the trigger signal] Initial data: DELAY_F[23..0] = 0, data range: 0 to 99 Sets the delay time (in useconds) that is from the trigger signal input to the start of the exposure
58H: FPS_I[7..0] 59H: FPS_I[15..8]	[Frame rate (Hz, integer)] Initial data: FPS_F[15..0] = 89, data range: 0 to 360 Sets the frame rate as Hz. Frame rate = (FPS_I[15..0]). (FPS_F[23..0]) Hz Frame Rate Range: 0.72028 to 360.33325 Hz Max frame rate for full resolution: 89.91172 Hz (as initial data)

<table>
<tr><th>Command No.</th><th>Command Descriptions</th></tr>
<tr><td>5AH: FPS_F[7..0]
5BH: FPS_F[15..8]
5CH: FPS_F[23..16]</td><td>[Frame rate (Hz, decimal)]
Initial data: FPS_F[23..0] = 91,172, FPS_I[15..0], data range: 0 to 99,999
This sets the frame rate as Hz.

Frame rate = (FPS_I[15..0]). (FPS_F[23..0]) Hz</td></tr>
<tr><td>78H: TESTP[7..0]</td><td>[Test pattern selection] Initial data: TESTP[7..0] = 00H
This sets the test pattern output from the camera.
D[7..0]
D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0

<u>00H: Video Output</u> 01H: Gray Scale
02H: Ramp Wave 03H: 100% White
04H: White Clip 05H: Color bar (RGB Bayer)
Others: Black</td></tr>
<tr><td>79H: EFFCT[7..0]</td><td>[Image effect selection] Initial data: EFFCT[7..0] = 00H
This sets the image effect.
D[7..0]
D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0

D7: Negative video / Positive video selection <u>0: Positive Image</u> 1: Negative image
D6 to D0: Image Effect <u>00H: No effect (Original)</u> 01H: 9bit gradation
02H: 8bit gradation 03H: 7bit gradation
04H: 6bit gradation 05H: 5bit gradation
06H: 4bit gradation 07H: 3bit gradation
08H: 2bit gradation 09H: 1bit gradation
0A to 7FH: No Function
(Prohibited setting. Do not set these values)</td></tr>
<tr><td>80H: E2P[7..0]</td><td>[EEPROM control] Initial data: e2p[7..0] = 00H
D[7..0]
D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0

D7 to D1: No function <u>Always set as “0000000”</u>
D0: Write control to the EEPROM <u>0: Prohibited</u> 1: Accept

Note: This bit is cleared to “0” automatically by the internal process after the execution of the command.</td></tr>
</table>

<table>
<tr><th>Command No.</th><th>Command Descriptions</th></tr>
<tr><td>F0H: OUTSEL[7..0]</td><td>[The output signal selection for the power/IO connector] Initial data: OUTSEL[7..0] = 20H
Sets the output signal from the power/IO connector.
D[7..0]
<table>
<tr><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td></tr>
</table>

D7 to D4: Output signal for the 4pin of the power/IO connector
0: FrameTriggerWait signal
1: UserOutput signal
<u>2: ExposureActive signal</u>
3: TriggerAuxiliary signal
4: TriggerInternal signal (after mask and delay process)
5: SensorReadOut signal
6 to F: No function (Prohibited settings. Do not set these values)
D3 to D0: Output signal for the 3pin of the power/IO connector
<u>0: FrameTriggerWait signal</u>
1: UserOutput signal
2: ExposureActive signal
3: TriggerAuxiliary signal
4: TriggerInternal signal (after mask and delay process)
5: SensorReadOut signal
6 to F: No function (Prohibited settings. Do not set these values)

Note: When “UserOutput signal” is selected, this sets the status of the signal with the “UserOutput signal for the power/IO connector (TEST2-D3,4)”.</td></tr>
<tr><td>F1H: TEST2[7..0]</td><td>[UserOutput signal for the power/IO connector] Initial data: TEST2[7..0] = 00H
This sets the status of the UserOutput signal.
D[7..0]
<table>
<tr><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td></tr>
</table>

D7: UserOutput signal for the 7pin of the power/IO connector <u>0: Low</u> 1: High
D6: UserOutput signal for the 6pin of the power/IO connector <u>0: Low</u> 1: High
D5: UserOutput signal for the 5pin of the power/IO connector <u>0: Low</u> 1: High
D4: UserOutput signal for the 4pin of the power/IO connector <u>0: Low</u> 1: High
D3: UserOutput signal for the 3pin of the power/IO connector <u>0: Low</u> 1: High
D2 to D0: No function <u>Always set as “000”</u>

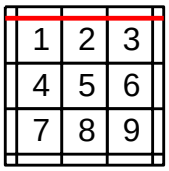
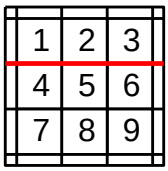
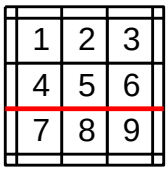
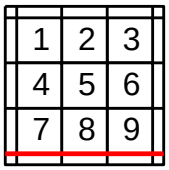
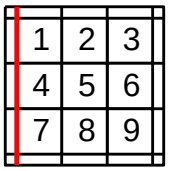
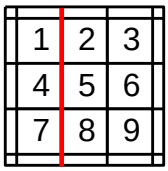
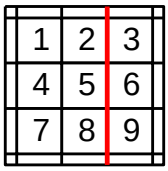
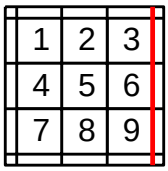
Note: The UserOutput signal is enabled when the “UserOutput signal” is selected at the “Output signal selection (OUTSEL)”.</td></tr>
</table>

Command No.	Command Descriptions
F8H: OUTSEL1[7..0]	[The output signal selection for the power/IO connector] Initial data: OUTSEL1[7..0] = 00H Sets the output signal from the power/IO connector. D[7..0] D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 D7 to D4: Output signal for the 6pin of the power/IO connector 0: FrameTriggerWait signal 1: UserOutput signal 2: ExposureActive signal 3: TriggerAuxiliary signal 4: TriggerInternal signal (after mask and delay process) 5: SensorReadOut signal 6 to F: No function (Prohibited settings. Do not set these values) D3 to D0: Output signal for the 5pin of the power/IO connector 0: FrameTriggerWait signal 1: UserOutput signal 2: ExposureActive signal 3: TriggerAuxiliary signal 4: TriggerInternal signal (after mask and delay process) 5: SensorReadOut signal 6 to F: No function (Prohibited settings. Do not set these values) Note: When “UserOutput signal” is selected, this sets the status of the signal with the “UserOutput signal for the power/IO connector (TEST2-D3,4)”.
F9H: OUTSEL2[7..0]	[The output signal seletion for the power/IO connector] Initial data: OUTSEL2[7..0] = 00H This sets the output signal from the power/IO connector. D[7..0] D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 D7 to D4: No function Always set as “0000” D3 to D0: Output signal for the 7pin of the power/IO connector 0: FrameTriggerWait signal 1: UserOutput signal 2: ExposureActive signal 3: TriggerAuxiliary signal 4: TriggerInternal signal (after mask and delay process) 5: SensorReadOut signal 6 to F: No function (Prohibited settings. Do not set these values) Note: When “UserOutput signal” is selected, this sets the status of the signal with the “UserOutput signal for the power/IO connector (TEST2-D3,4)”.

3. Description of the Camera Control Commands (Device Code: 100000)
The underlined settings are the factory default settings.

Command No.	Command Descriptions
18H:[7..0]	[JTAG for the user configurable FPGA] Initial data: 00H This sets the JTAG connection ON/OFF for the user configurable FPGA. D[7..0] D7 D6 D5 D4 D3 D2 D1 D0 D7 to D1: No Function Always set as "0000000" D0: JTAG 0: OFF 1: ON
19H: [7..0]	[The user configurable FPGA enable] Initial data: 00H This sets the user configurable FPGA as ENABLE/DISABLE when the camera is started up. D[7..0] D7 D6 D5 D4 D3 D2 D1 D0 D7 to D1: No Function Always set as "0000000" D0: User Configurable FPGA 0: Disable 1: Enable
20H: [7..0]	[Exposure Mode] Initial data: 00H This sets the exposure mode (the AGC), the shutter mode and the iris lens control method. D[7..0] D7 D6 D5 D4 D3 D2 D1 D0 D7 to D4: No function Always set as "0000" D3: AGC 0: OFF (Fixed gain) 1: ON (AGC) D2: Shutter Mode 0: OFF (Fixed shutter) 1: ON (Auto shutter) D1: Iris Lens Control Method 0: OFF (Manual control) 1: ON (Auto control) D0: No Function Always set as "0"
21H: [7..0]	[AGC maximum limit] Initial data: 255, data range: 0 to 255 Sets the maximum limit for the AGC.
23H: [7..0] 24H: [15..8] 25H: [20,,16]	[The upper limit for the electronic shutter for the auto shutter] Initial data: 11,122, data range: 0 to 1,048,575 This sets the upper limit of the electronic shutter for the auto shutter as usecond.
26H: [7..0] 27H: [15..8] 28H: [20,,16]	[The lower limit for the electronic shutter for the auto shutter] Initial data: 0, data range: 0 to 1,048,575 This sets the lower limit of the electronic shutter for the auto shutter as usecond.
29H: [7..0]	[Weight1 for the ALC] Initial data: 11H This sets the weight for the ALC weight area 1 and 2. D[7..0] D7 D6 D5 D4 D3 D2 D1 D0 D7 to D4: Weight for ALC weight area 2 1 Range: 0 to 15 D3 to D0: Weight for ALC weight area 1 1 Range: 0 to 15 *Please set the ALC weight area with "30H to 3FH".

Command No.	Command Descriptions
2AH:[7..0]	[Weight2 for the ALC] Initial data: 11H This sets the weight for the ALC weight area 3 and 4. D[7..0] D7 D6 D5 D4 D3 D2 D1 D0 D7 to D4: Weight for ALC weight area 4 1 Range: 0 to 15 D3 to D0: Weight for ALC weight area 3 1 Range: 0 to 15 *Please set the ALC weight area with “30H to 3FH”.
2BH:[7..0]	[Weight3 for the ALC] Initial data: 1AH This sets the weight for the ALC weight area 5 and 6. D[7..0] D7 D6 D5 D4 D3 D2 D1 D0 D7 to D4: Weight for ALC weight area 6 1 Range: 0 to 15 D3 to D0: Weight for ALC weight area 5 1 Range: 0 to 15 *Please set the ALC weight area with “30H to 3FH”.
2CH:[7..0]	[Weight4 for the ALC] Initial data: 11H This sets the weight for the ALC weight area 7 and 8. D[7..0] D7 D6 D5 D4 D3 D2 D1 D0 D7 to D4: Weight for ALC weight area 8 1 Range: 0 to 15 D3 to D0: Weight for ALC weight area 7 1 Range: 0 to 15 *Please set the ALC weight area with “30H to 3FH”.
2DH:[7..0]	[Weight5 for the ALC] Initial data: 01H This sets the weight for the ALC weight area 9. D[7..0] D7 D6 D5 D4 D3 D2 D1 D0 D7 to D4: No Function Always set as “0000” D3 to D0: Weight for ALC weight area 9 1 Range: 0 to 15 *Please set the ALC weight area with “30H to 3FH”.
2EH:[7..0]	[Target brightness for ALC] Initial data: 128, data range: 0 to 255 This sets the target brightness for the ALC function (AGC, auto shutter or iris lens auto control).
2FH:[7..0]	[ALC peak-average] Initial data: 0, data range: 0 to 255 This sets the control standard for the ACL function (AGC, auto shutter or iris lens auto control) When set as 0 (the Average is 100% and Peak is 0%) the ALC functions with the average brightness of the photometry area. When set as 255 (the Average is 0% and the Peak is 100%) the ALC functions with the peak brightness of the photometry area.

Command No.	Command Descriptions
30H:[7..0] 31H:[15..8]	[Vertical_1 position for the ALC weight area] Initial data: 32, data range: 0 to 493 This sets the vertical 1 position for the ALC weight area. 
32H:[7..0] 33H:[15..8]	[Vertical_2 position for the ALC weight area] Initial data: 169, data range: 0 to 493 This sets the vertical 2 position for the ALC weight area. 
34H:[7..0] 35H:[15..8]	[Vertical_3 position for the ALC weight area] Initial data: 298, data range: 0 to 493 This sets the vertical 3 position for the ALC weight area. 
36H:[7..0] 37H:[15..8]	[Vertical_4 position for the ALC weight area] Initial data: 462, data range: 0 to 493 This sets the vertical 4 position for the ALC weight area. 
38H:[7..0] 39H:[15..8]	[Horizontal _1 position for the ALC weight area] Initial data: 36, data range: 0 to 647 This sets the horizontal 1 position for the ALC weight area. 
3AH:[7..0] 3BH:[15..8]	[Horizontal _2 position for the ALC weight area] Initial data: 252, data range: 0 to 647 This sets the horizontal 2 position for the ALC weight area. 
3CH:[7..0] 3DH:[15..8]	[Horizontal _3 position for the ALC weight area] Initial data: 396, data range: 0 to 647 This sets the horizontal 3 position for the ALC weight area. 
3EH:[7..0] 3FH:[15..8]	[Horizontal_4 position for the ALC weight area] Initial data: 612, data range: 0 to 647 This sets the horizontal 4 position for the ALC weight area. 

<table>
<tr><th>Command No.</th><th>Command Descriptions</th></tr>
<tr><td>40H:[7..0]</td><td>[White balance mode] Initial data: 00H
This sets the white balance mode for the color camera.
D[7..0]
<table>
<tr><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td></tr>
</table>

D7 to D4: No function — Always set as “0000”
D3: Push to set white balance operation — 0: OFF 1: ON
D2 to D0: White balance mode — 000: OFF 001: Preset 1 010: Preset 2 011: Preset 3, 100: Auto white balance 101: Push to set white balance 110 to 111: No function
(Prohibited settings – Do not set these values)

*When using the push-to-set white balance, set the white balance mode as “Push to set white balance” then change “0” to “1” for the push-to-set white balance operation.</td></tr>
<tr><td>41H: GainR1 [7..0]</td><td>[Preset_1 white balance (Red gain)] Initial data: 0, data range: 0 to 255
Sets the Red gain for the preset_1 white balance.

Red of the camera output image data = (CCD_R –CLAMP Level) x (1 + GainR1[7..0]/64) + CLAMP Level

*CCD_R: Red of the CCD output image data
*CLAMP Level: Clamp level (The calculated value of 38H)</td></tr>
<tr><td>42H: GainGr1 [7..0]</td><td>[Preset_1 white balance (Gr gain)] Initial data: 0, data range: 0 to 255
Sets the Gr gain for the preset_1 white balance.

Gr of the camera output image data = (CCD_Gr – CLAMP Level) x (1 + GainGr1[7..0]/64) + CLAMP Level

*CCD_Gr: Gr of the CCD output image data
*CLAMP Level: Clamp level (The calculated value of 38H)</td></tr>
<tr><td>43H: GainB1 [7..0]</td><td>[Preset_1 white balance (Blue gain)] Initial data: 0, data range: 0 to 255
Sets the Blue gain for the preset_1 white balance.

Blue of the camera output image data = (CCD_B – CLAMP Level) x (1 + GainB1[7..0]/64) + CLAMP Level

*CCD_B: Blue of the CCD output image data
*CLAMP Level: Clamp level (The calculated value of 38H)</td></tr>
<tr><td>44H: GainGb1 [7..0]</td><td>[Preset_1 white balance (Gb gain)] Initial data: 0, data range: 0 to 255
Sets the Gb gain for the preset_1 white balance.

Gb of the camera output image data = (CCD_Gb – CLAMP Level) x (1 + GainGb1[7..0]/64) + CLAMP Level

*CCD_Gb: Gb of the CCD output image data
*CLAMP Level: Clamp level (The calculated value of 38H)</td></tr>
</table>

Command No.	Command Descriptions
45H: GainR2 [7..0]	[Preset_2 white balance (Red gain)] Initial data: 0, data range: 0 to 255 Sets the Red gain for the preset_2 white balance. Red of the camera output image data = (CCD_R –CLAMP Level) x (1 + GainR2[7..0]/64) + CLAMP Level *CCD_R: Red of the CCD output image data *CLAMP Level: Clamp level (The calculated value of 38H)
46H: GainGr2 [7..0]	[Preset_2 white balance (Gr gain)] Initial data: 0, data range: 0 to 255 Sets the Gr gain for the preset_2 white balance. Gr of the camera output image data = (CCD_Gr – CLAMP Level) x (1 + GainGr2[7..0]/64) + CLAMP Level *CCD_Gr: Gr of the CCD output image data *CLAMP Level: Clamp level (The calculated value of 38H)
47H: GainB2 [7..0]	[Preset_2 white balance (Blue gain)] Initial data: 0, data range: 0 to 255 Sets the Blue gain for the preset_2 white balance. Blue of the camera output image data = (CCD_B – CLAMP Level) x (1 + GainB2[7..0]/64) + CLAMP Level *CCD_B: Blue of the CCD output image data *CLAMP Level: Clamp level (The calculated value of 38H)
48H: GainGb2 [7..0]	[Preset_2 white balance (Gb gain)] Initial data: 0, data range: 0 to 255 Sets the Gb gain for the preset_2 white balance. Gb of the camera output image data = (CCD_Gb – CLAMP Level) x (1 + GainGb2[7..0]/64) + CLAMP Level *CCD_Gb: Gb of the CCD output image data *CLAMP Level: Clamp level (The calculated value of 38H)
49H: GainR3 [7..0]	[Preset_3 white balance (Red gain)] Initial data: 0, data range: 0 to 255 Sets the Red gain for the preset_3 white balance. Red of the camera output image data = (CCD_R –CLAMP Level) x (1 + GainR3[7..0]/64) + CLAMP Level *CCD_R: Red of the CCD output image data *CLAMP Level: Clamp level (The calculated value of 38H)
4AH: GainGr3 [7..0]	[Preset_3 white balance (Gr gain)] Initial data: 0, data range: 0 to 255 Sets the Gr gain for the preset_3 white balance. Gr of the camera output image data = (CCD_Gr – CLAMP Level) x (1 + GainGr3[7..0]/64) + CLAMP Level *CCD_Gr: Gr of the CCD output image data *CLAMP Level: Clamp level (The calculated value of 38H)

Command No.	Command Descriptions
4BH: GainB3 [7..0]	[Preset_3 white balance (Blue gain)] Initial data: 0, data range: 0 to 255 Sets the Blue gain for the preset_3 white balance. Blue of the camera output image data = (CCD_B – CLAMP Level) x (1 + GainB3[7..0]/64) + CLAMP Level *CCD_B: Blue of the CCD output image data *CLAMP Level: Clamp level (The calculated value of 38H)
4CH: GainGb3 [7..0]	[Preset_3 white balance (Gb gain)] Initial data: 0, data range: 0 to 255 Sets the Gb gain for the preset_3 white balance. Gb of the camera output image data = (CCD_Gb – CLAMP Level) x (1 + GainGb3[7..0]/64) + CLAMP Level *CCD_Gb: Gb of the CCD output image data *CLAMP Level: Clamp level (The calculated value of 38H)
4EH: [7..0] 4FH: [15..8]	[Bright level threshold for auto white balance process] Initial data: 3072, data range: 0 to 4095 This sets the bright level threshold for the auto white balance process. The auto white balance process uses the color information of the pixel (when the brightness of the pixel is greater than this value)
50H: [7..0] 51H: [15..8]	[Y_offset for AOI] Initial data: 0, data range: 4 ≤ “Y_offset + Height” ≤ 494 Sets the Y_offset (the vertical start position of the image for the AOI)
52H: [7..0] 53H: [15..8]	[Height for AOI] Initial data: 494, data range: 4 ≤ “Y_offset + Height” ≤ 494 Sets the height (the vertical size of the image for the AOI)
54H: [7..0] 55H: [15..8]	[X_offset for AOI] Initial data: 0, data range: 8 ≤ “X_offset + Width” ≤ 648 Sets the X_offset (the horizontal start position of the image for the AOI)
56H: [7..0] 57H: [15..8]	[Width for AOI] Initial data: 648, data range: 8 ≤ “X_offset + Width” ≤ 648 Sets the width (the horizontal size of the image for the AOI)
58H: [7..0] 59H: [15..8]	[Vertical_1 position for the white balance area] Initial data: 0, data range: 0 to 493 This sets the vertical 1 position (the vertical start position for the white balance area). This is used for the gain calculation for the auto white balance and the push-to-set white balance.
5AH: [7..0] 5BH: [15..8]	[Vertical_2 position for the white balance area] Initial data: 493, data range: 0 to 493 This sets the vertical 2 position (the vertical start position for the white balance area). This is used for the gain calculation for the auto white balance and the push-to-set white balance.
5CH: [7..0] 5DH: [15..8]	[Horizontal_1 position for the white balance area] Initial data: 0, data range: 0 to 647 This sets the horizontal 1 position (the horizontal start position for the white balance area). This is used for the gain calculation for the auto white balance and the push-to-set white balance.

<table>
<tr><th>Command No.</th><th>Command Descriptions</th></tr>
<tr><td>5EH: [7..0]
5FH: [15..8]</td><td>[Horizontal_2 position for the white balance area]
Initial data: 647, data range: 0 to 647
This sets the horizontal 2 position (the horizontal start position for the white balance area).
This is used for the gain calculation for the auto white balance and the push-to-set white balance.</td></tr>
<tr><td>60H: [7..0]</td><td>[Camera mode 1] Initial data: 00H
Sets the white balance area ON/OFF and the gamma table ON/OFF
D[7..0]
<table>
<tr><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td></tr>
</table>
<table>
<tr><td>D7 to D5:</td><td>No function</td><td>Always set as “000”</td><td></td></tr>
<tr><td>D4:</td><td>White balance area ON/OFF</td><td>0: OFF(Full screen)</td><td>1: ON(setup area)</td></tr>
<tr><td>D3 to D1:</td><td>No function</td><td>Always set as “000”</td><td></td></tr>
<tr><td>D0:</td><td>Gamma table ON/OFF</td><td>0: OFF (Gamma=1.0)</td><td>1: ON</td></tr>
</table></td></tr>
<tr><td>80H:
GainRP[7..0]</td><td>[Push to set white balance (Red gain)] Initial data: 0, data range: 0 to 255
This sets the Red gain for the Push to set white balance.

Red of the camera output image data = (CCD_R – CLAMP Level) x (1 + GainRP[7..0] / 64) + CLAMP Level

*CCD_R: Red of the CCD output image data
*CLAMP Level: Clamp level (The calculated value of 38H)</td></tr>
<tr><td>81H:
GainGrP[7..0]</td><td>[Push to set white balance (Gr gain)] Initial data: 0, data range: 0 to 255
This sets the Gr gain for the Push to set white balance.

Gr of the camera output image data = (CCD_Gr – CLAMP Level) x (1 + GainGrP[7..0] / 64) + CLAMP Level

*CCD_Gr: Gr of the CCD output image data
*CLAMP Level: Clamp level (The calculated value of 38H)</td></tr>
<tr><td>82H:
GainBR[7..0]</td><td>[Push to set white balance (Blue gain)] Initial data: 0, data range: 0 to 255
This sets the Blue gain for the Push to set white balance.

Blue of the camera output image data = (CCD_B – CLAMP Level) x (1 + GainBR[7..0] / 64) + CLAMP Level

*CCD_B: Blue of the CCD output image data
*CLAMP Level: Clamp level (The calculated value of 38H)</td></tr>
<tr><td>83H:
GainGbP[7..0]</td><td>[Push to set white balance (Gb gain)] Initial data: 0, data range: 0 to 255
This sets the Gb gain for the Push to set white balance.

Gb of the camera output image data = (CCD_Gb – CLAMP Level) x (1 + GainGbP[7..0] / 64) + CLAMP Level

*CCD_Gb: Gb of the CCD output image data
*CLAMP Level: Clamp level (The calculated value of 38H)</td></tr>
<tr><td>90H:[7..0]</td><td>[Iris lens adjustment] Initial data: 80, data range: 0 to 255
This sets the driving voltage of the iris lens for the iris lens auto control.</td></tr>
</table>

Command No.	Command Descriptions
92H: [7..0]	[Iris lens manual adjustment] Initial data: 01H This sets the iris lens manual adjustment operation. D[7..0] D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 D7 to D3: No function — Always set as "000000" D1 to D0: Manual adjustment operation — 00: Hold; 01: Open; 10: Close; 11: No function (Prohibited settings. Do not set these values)
C0H: [7..0]	[Image data between FPGAs] Initial data: 00H D[7..0] D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 D7 to D6: No function — Always set as "00" D5 to D4: Image process after the image data from the user configurable FPGA 00: No process (No data from the user FPGA) (No data from the user configurable FPGA) 01: White balance, gamma and color interpolation 10: Gamma and color interpolation 11: Color interpolation D3 to D2: No function — Always set as "00" D1 to D0: Image data from Sentech FPGA to the user configurable FPGA 00: CCD out image data 01: White balance processed image data 10: White balance and gamma processed image data 11: No function (Prohibited setting. Do not set these values) Note: White balance and color interpolation process are available only for color camera.
C1H: [7..0]	[Output the signal selection] Initial data: 00H D[7..0] D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 D7 to D5: No function — Please set as "000" D4: Output signal for 7 pin (Out4) of the power/IO connector — 0: Output signal from Sentech FPGA; 1: Output signal from the user configurable FPGA D3: Output signal for 6 pin (Out3) of the power/IO connector — 0: Output signal from Sentech FPGA; 1: Output signal from the user configurable FPGA D2: Output signal for 5 pin (Out3) of the power/IO connector — 0: Output signal from Sentech FPGA; 1: Output signal from the user configurable FPGA D1: Output signal for 4 pin (Out3) of the power/IO connector — 0: Output signal from Sentech FPGA; 1: Output signal from the user configurable FPGA D0: Output signal for 3 pin (Out3) of the power/IO connector — 0: Output signal from Sentech FPGA; 1: Output signal from the user configurable FPGA Note: When "Output signal from SentechFPGA" is selected, this selects the output signal from the Sentech FPGA for the power/IO connector with the "Output signal selection (F0H, F8H and F9H)".

4. Sequence for Saving the Command to the EEPROM
   Please use the following sequence for commands to save to the EEPROM.

   a. Set “1” to the 80H.0 to accept the “write control to the EEPROM”.
   b. Send the command and the save data with the EEPROM access command, this sets “1” for the page selection.
   c. The camera sends back one of the following receiving codes after writing the EEPROM.
      01H: OK
      17H: EEPROM write error
   d. 80H.0 automatically changes to “0” after writing the EEPROM.

   Notes:
   - Do NOT save to the EEPROM when “0” is set to 80H.0
   - When saving a multiple sequence command to the EEPROM, the data is saved to the EEPROM by executing steps a~d one time.
     An example of a multiple sequence command is: “10H, 11H, 12H and 13H” or “22H, 23H and 24H”.
   - When saving multiple command data (that are not a sequence command) to the EEPROM, it is necessary to execute steps a~d the same number of times as the command data.

E. GenICam command / Camera Command Reference Table

GenICam command	Camera command		
	Device	Command	Function
Width	100000	56-57H	Width for AOI
Height	100000	52-53H	Height for AOI
PixelFormat	000000	12H.6-7	Video out
OffsetX	100000	54-55H	X offset for AOI
OffsetY	100000	50-51H	Y offset for AOI
ExposureMode	000000	10H.5	Trigger mode
ExposureTimeRaw	000000	20-22H	Exposure time of the electronic shutter
ExposureAuto	100000	20H.2	Shutter mode
AcquistionFrameRate	000000	58-5CH	Frame rate
TriggerDelay	000000	50-53H	The delay time for the trigger signal
TriggerActivation	000000	10H.6	Trigger polarity
TriggerSource	000000	12H.5	Trigger signal type
TriggerSoftware	000000	16H.0	Generate command software trigger
TriggerSoftwareSource	000000	16H.6-7	Software trigger source selection
TriggerMode	000000	11H.3	Function mode
LineSource0	000000	F0H.0-3	Output signal for 3 pin of the power/IO connector
LineSource1	000000	F0H.4-7	Output signal for 4 pin of the power/IO connector
LineSource2	000000	F8H.0-3	Output signal for 5 pin of the power/IO connector
LineSource3	000000	F8H.4-7	Output signal for 6 pin of the power/IO connector
LineSource4	000000	F9H.0-3	Output signal for 7 pin of the power/IO connector
UserOutputValue0	000000	F1H.3	UserOutput signal for 3 pin of the power/IO connector
UserOutputValue1	000000	F1H.4	UserOutput signal for 4 pin of the power/IO connector
UserOutputValue2	000000	F1H.5	UserOutput signal for 5 pin of the power/IO connector
UserOutputValue3	000000	F1H.6	UserOutput signal for 6 pin of the power/IO connector
UserOutputValue4	000000	F1H.7	UserOutput signal for 7 pin of the power/IO connector
BalanceWhiteAuto	100000	40H.0-2	White balance mode
BalanceRatio_R_Preset1	100000	41H	Preset1 white balance (Red gain)
BalanceRatio_Gr_Preset1	100000	42H	Preset1 white balance (Gr gain)
BalanceRatio_B_Preset1	100000	43H	Preset1 white balance (Blue gain)
BalanceRatio_Gb_Preset1	100000	44H	Preset1 white balance (Gb gain)

GenICam command	Camera command		
	Device	Command	Function
BalanceRatio_R_Preset2	100000	45H	Preset2 white balance (Red gain)
BalanceRatio_Gr_Preset2	100000	46H	Preset2 white balance (Gr gain)
BalanceRatio_B_Preset2	100000	47H	Preset2 white balance (Blue gain)
BalanceRatio_Gb_Preset2	100000	48H	Preset2 white balance (Gb gain)
BalanceRatio_R_Preset3	100000	49H	Preset3 white balance (Red gain)
BalanceRatio_Gr_Preset3	100000	4AH	Preset3 white balance (Gr gain)
BalanceRatio_B_Preset3	100000	4BH	Preset3 white balance (Blue gain)
BalanceRatio_Gb_Preset3	100000	4CH	Preset3 white balance (Gb gain)
BalanceRatio_R_Once	100000	80H	Push to set white balance (Red gain)
BalanceRatio_Gr_Once	100000	81H	Push to set white balance (Gr gain)
BalanceRatio_B_Once	100000	82H	Push to set white balance (Blue gain)
BalanceRatio_Gb_Once	100000	83H	Push to set white balance (Gb gain)
GainAuto	100000	20H.3	AGC
GainRaw	000000	30H	CDS gain
SmearHalfReduction	000000	11H.4	Smear half reduction
ReloadGammaData	100000	60H.7	Gamma table ON/OFF
LensManualAdjustment	100000	92H.0-1	Iris lens manual adjustment operation
LensIrisAdjustment	100000	90H	Iris lens adjustment
ALCIrisLens	100000	20H.1	Iris lens control method
Min_ShutterTime	100000	26-28H	The lower limit of the electronic shutter for auto shutter
Max_ShutterTime	100000	23-25H	The upper limit of the electronic shutter for auto shutter
AGCRange	100000	21H	AGC maximum limit
TargetBrightness	100000	2EH	Target brightness for ALC
ALC_Peak_Average	100000	2FH	ALC peak-average
DigitalGain	000000	31H	The digital gain

GenICam command	Camera command		
	Device	Command	Function
ALCWeight1	100000	29H.0-3	Weight1 for ALC
ALCWeight2	100000	29H.4-7	Weight2 for ALC
ALCWeight3	100000	2AH.0-3	Weight3 for ALC
ALCWeight4	100000	2AH.4-7	Weight4 for ALC
ALCWeight5	100000	2BH.0-3	Weight5 for ALC
ALCWeight6	100000	2BH.4-7	Weight6 for ALC
ALCWeight7	100000	2CH.0-3	Weight7 for ALC
ALCWeight8	100000	2CH.4-7	Weight8 for ALC
ALCWeight9	100000	2DH.0-3	Weight9 for ALC
ALCWindowV1	100000	30-31H	Vertical1 position for the ALC weight area
ALCWindowV2	100000	32-33H	Vertical2 position for the ALC weight area
ALCWindowV3	100000	34-35H	Vertical3 position for the ALC weight area
ALCWindowV4	100000	36-37H	Vertical4 position for the ALC weight area
ALCWindowH1	100000	38-39H	Horizontal1 position for the ALC weight area
ALCWindowH2	100000	3A-3BH	Horizontal2 position for the ALC weight area
ALCWindowH3	100000	3C-3DH	Horizontal3 position for the ALC weight area
ALCWindowH4	100000	3E-3FH	Horizontal4 position for the ALC weight area
WB_WindowH1	100000	58-59H	Vertical1 position for the white balance area
WB_WindowH2	100000	5A-5BH	Vertical2 position for the white balance area
WB_WindowV1	100000	5C-5DH	Horizontal1 position for the white balance area
WB_WindowV2	100000	5E-5FH	Horizontal2 position for the white balance area
WB_WindowMode	100000	60H.4	White balance area ON/OFF
YThreshold	100000	4E-4FH	Bright level threshold for auto white balance
ALCWeight4	100000	2AH.4-7	Weight4 for ALC
ALCWeight5	100000	2BH.0-3	Weight5 for ALC

Caution:
Width, Height and PixelFormat all affect the image data size.
Therefore, please use the GenICam command name command when changing these values, similar to the sample code below:

As an example, changing the Width:

```
BOOL SetWidth( PvDevice *pDevice, PvInt64 lValue )
{
    PvGenInteger* lGenInteger = dynamic_cast<PvGenInteger*>( pDevice->GetGenParameters()->Get( "Width" ) );
    PvResult lResult = lGenInteger->SetValue(lValue);
    return lResult.IsOK();
}
```

Revision

Rev	Date	Changes	Notes
1.00	2011/09/21	New Document	

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